Exhibit 4

[redacted]

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Paper 49
Entered: December 6, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,[1]
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00996
Patent 11,016,918 B2

Before PATRICK M. BOUCHER, JON M. JURGOVAN, and DANIEL J. GALLIGAN, *Administrative Patent Judges.*

JURGOVAN, *Administrative Patent Judge*.

DECISION
Final Written Decision
Determining All Challenged Claims Unpatentable
Dismissing Petitioner's Motion to Exclude
35 U.S.C. § 318(a)

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[1] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and a petition in IPR2023-00406 and have been joined as petitioners in this proceeding. *See* Paper 26.

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Samsung") filed a Petition (Paper 1, "Pet.") for *inter partes* review of claims 1–30 ("challenged claims") of U.S. Patent 11,016,918 B2 (Ex. 1001, "the '918 patent"). Netlist, Inc. ("Patent Owner") filed a Preliminary Response (Paper 7, "Prelim. Resp.") to the Petition. We instituted *inter partes* review under 35 U.S.C. § 314(a). Paper 10 ("Inst. Dec.").

During the trial, Patent Owner filed a Response (Paper 21, "Resp."), Petitioner filed a Reply (Paper 25), and Patent Owner filed a Sur-Reply (Paper 31). We joined Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC as petitioners in this proceeding, and we refer to Samsung and these entities collectively as "Petitioner." *See* Paper 26.

Petitioner and Patent Owner requested oral argument (Papers 28 and 29). A hearing was conducted on September 11, 2023. Paper 47 ("Tr.").

Petitioner objected to evidence (Paper 32) and filed a Motion to Exclude (Paper 33). Patent Owner filed an Opposition to Petitioner's Motion to Exclude (Paper 34), and Petitioner filed a Reply (Paper 37) in support of its Motion to Exclude.

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). Having reviewed the complete trial record, we determine that Petitioner has shown, by a preponderance of the evidence, that the challenged claims are unpatentable.

II. BACKGROUND

A. Real Parties in Interest

The identified real parties in interest on the Petitioner side are the following entities: Samsung Electronics Co., Ltd., Samsung Semiconductor, Inc., Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC. Pet. 1; IPR2023-00406, Paper 3, 1.

Patent Owner identifies itself as the sole real party in interest. Paper 4, 1.

B. Related Matters

The parties advise that the '918 patent is related to the following pending matters:

- *Samsung Electronics Co., Ltd. et al. v Netlist, Inc.,* No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021)
- *Netlist, Inc. v. Micron Technology, Inc.*, No. 2:22-cv-00203 (E.D. Tex. filed June 13, 2022)
- IPR2012-00999 (U.S. Patent No. 11,232,054)
- U.S. Patent Application No. 17/582,797

Pet. 1; Paper 4, 1; Paper 9, 2; Paper 12, 1.

The parties advise that the following related proceeding is no longer pending:

- IPR2017-00692 (U.S. Patent No. 8,874,831)

Pet. 1; Paper 4, 1.

C. Overview of the '918 Patent (Ex. 1001)

The '918 patent is titled "Flash-DRAM Hybrid Memory Module." Ex. 1001, code (54). Figure 12 of the '918 patent is reproduced below.

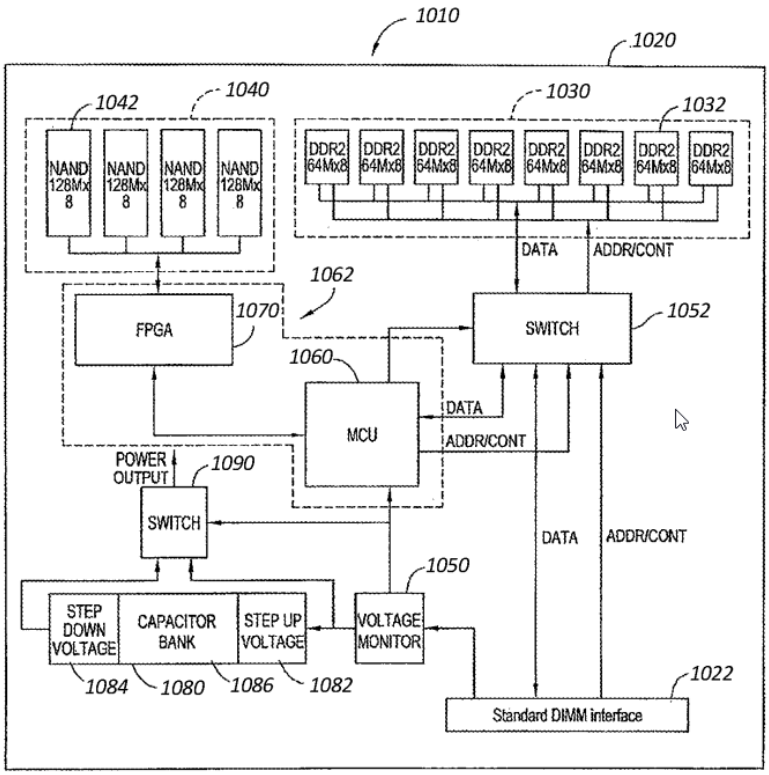


FIG. 12

Figure 12 shows an example memory system 1010 of the '918 patent. *Id.* at 21:14–16. The memory system 1010 includes a volatile memory subsystem 1030, a non-volatile memory subsystem 1040, and a controller 1062 operatively coupled to the volatile memory subsystem 1030 and selectively coupled to the non-volatile memory subsystem 1040. *Id.* at 21:16–22. Volatile memory 1030 may comprise elements 1032 of two or more dynamic random access memory (DRAM) elements such as double data rate (DDR), DDR2, DDR3, and synchronous DRAM (SDRAM). *Id.* at 22:16–19. Non-volatile memory 1040 may comprise elements 1042 of flash memory elements such as NOR, NAND, ONE-NAND flash and multi-level

cell (MLC). *Id.* at 22:35–40. Memory system 1010 may comprise a memory module or printed circuit board (PCB) 1020. *Id.* at 21:24–26. Memory system 1010 has an interface 1022 for power voltage, data, address, and control signal transfer between memory system 1010 and a host system. *Id.* at 22:3–6.

Controller 1062 may include microcontroller unit 1060 and FPGA logic 1070, either as separate devices or integrated together. *Id.* at 24:35–37, 23:19–22, Fig. 14. Microcontroller 1060 may transfer data between the volatile memory 1030 and non-volatile memory 1040. *Id.* at 24:35–41. Logic element 1070 provides signal level translation and address translation between the volatile memory and the non-volatile memory. *Id.* at 24:45–56.

When the system is operating normally, controller 1062 controls switch 1052 to decouple the volatile memory 1030 from controller 1062 and the non-volatile memory 1040 (the '918 patent refers to this as the "first state."). *Id.* at 24:60–25:7. In response to a power interruption, for example, controller 1062 controls switch 1052 to couple the volatile memory 1030 to itself and non-volatile memory 1040, and transfers data from the volatile memory to the non-volatile memory to prevent its loss (the '918 patent refers to this as the "second state"). *Id.* at 25:9–20.

Memory system 1010 may comprise a voltage monitor 1050 to monitor voltage supplied from the host system via interface 1022. *Id.* at 25:8–10. When the voltage monitor 1050 detects a low voltage condition, the voltage monitor transmits a signal to the controller 1062 to indicate the detected condition. *Id.* at 25:11–15.

Power may be supplied from a first power supply (e.g., a system power supply) when the memory system 1010 is in the first state and from a

second power supply 1080 when the memory system 1010 is in the second state. *Id.* at 25:54–58. Second power supply 1080 may comprise step-up transformer 1082, step-down transformer 1084, and capacitor bank 1086 with one or more capacitors. *Id.* at 26:3–13.

The memory system 1010 further has a third state in which controller 1062 is decoupled from the volatile memory system 1030 and power is supplied to the volatile memory subsystem 1030 from a third power supply (not shown). *Id.* at 25:62–69. "[T]he third power supply may provide power to the volatile memory subsystem 1030 when the memory system 1010 detects that a trigger condition is likely to occur but has not yet occurred." *Id.* at 25:66–26:3.

Figure 16 of the '918 patent is reproduced below.

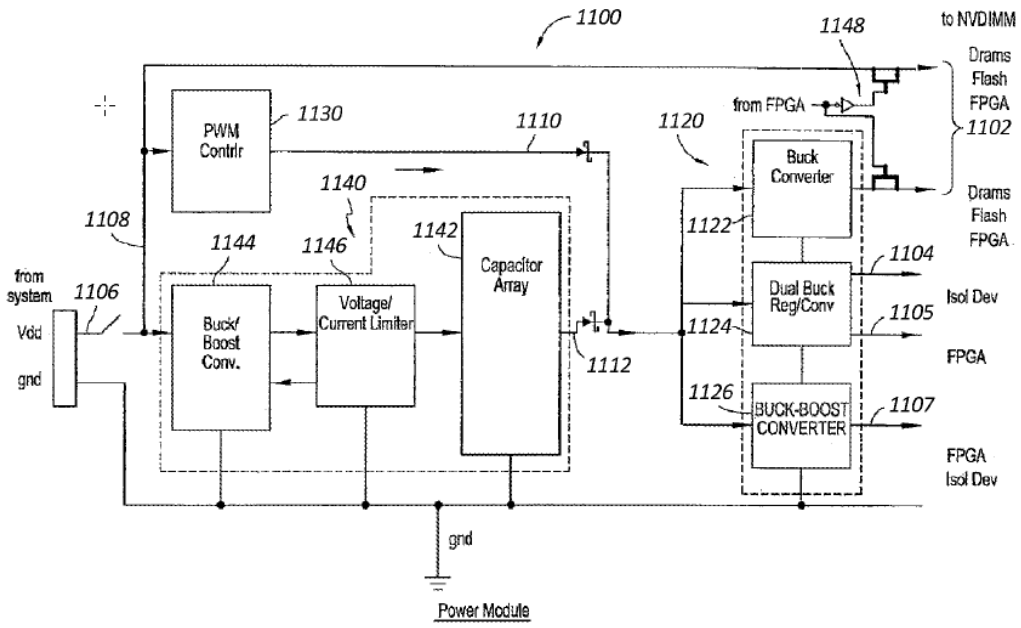


FIG. 16

Figure 16 shows power module 1100 of memory system 1010. *Id.* at 27:59–61. Power module 1100 comprises conversion element 1120, first power element 1130, and second power element 1140. *Id.* at 28:7–15,

28:20–22. Conversion element 1120 comprises sub-blocks 1122, 1124, 1126 comprised of various converter circuits such as buck converters, boost converters, and buck-boost converters for providing various voltages 1102, 1104, 1105, 1107 from the outputs of the first and second power elements 1130, 1140. *Id.* at 29:18–54. The first power element 1130 may comprise a pulse-width modulation power controller generating voltage 1110 from voltages 1106, 1108. *Id.* at 28:13–15. Second power element 1140 may comprise capacitor array 1142, buck-boost converter 1144 receiving voltages 1106, 1108 and adjusting the voltage for charging the capacitor array, and voltage/current limiter 1146, which limits charge current to the capacitor array and stops charging the capacitor array 1142 when it reaches a certain charge voltage. *Id.* at 28:62–67. "[P]ower module 1100 provides power to [ ] components of the memory system 1010 using different elements based on a state of the memory system 1010 in relation to a trigger condition." *Id.* at 27:61–65.

Specifically, "[i]n a first state, the first voltage 1102 is provided to the memory system 1010 from the input 1106 and the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130." *Id.* at 28:27–31. "In a second state, the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120." *Id.* at 28:32–37. "In the third state, the fifth voltage 1112 is provided to the conversion element 1120 from the second power element 1140 and the first voltage 1104 is provided to the memory system 1010 from the conversion element 1120." *Id.* at 28:34–38. Transition from the first state to the second state may occur when power

module 1100 detects a power failure is about to occur, and transition from the second state to the third state may occur when it detects a power failure has occurred. *Id.* at 28:39–47.

D. Illustrative Claim

Of the challenged claims, claims 1, 16, and 23 are independent. Independent claim 1, reproduced below with brackets noting Petitioner's identifiers, is illustrative of the claimed subject matter.

> 1. [1.a] A memory module comprising:
> [1.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
> [1.c] a first buck converter configured to provide a first regulated voltage having a first voltage amplitude;
> [1.d] a second buck converter configured to provide a second regulated voltage having a second voltage amplitude;
> [1.e] a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;
> [1.f] a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and
> [1.g] a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:
> [1.h] a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and
> [1.i] [1.i.1] at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, [1.i.2] the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, [1.i.3] the at least one circuit coupled to both

> the second regulated voltage and the fourth regulated voltage, [1.i.4] wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.

Ex. 1001, 38:19–44.

E. Evidence

Petitioner relies on the following references (*see* Pet. 3, 10–14), as well as the Declaration of Dr. Andrew Wolfe (Ex. 1003).

Reference	Exhibit No.	Patent/Printed Publication
Harris	1023	U.S. Patent Pub. No. 2006/0174140 A1 to Harris, published August 3, 2006
Amidi	1024	U.S. Patent No. 7,724,604 B2, issued May 25, 2010
Spiers	1025	U.S. Patent Pub. No. 2006/0080515 A1, published April 13, 2006
FBDIMM Standards	1027, 1028	JESD82-20 and JESD205 standards published March 2007
Hajeck	1038	U.S. Patent No. 6,856,556 B1 to Hajeck, issued February 15, 2005

F. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–30 are unpatentable on the following Grounds (Pet. 3):

Claims Challenged	35 U.S.C. §	References
1–3, 8, 14, 15, 23	103(a)	Harris, FBDIMM Standards
1–30	103(a)	Harris, FBDIMM Standards, Amidi
1–30	103(a)	Harris, FBDIMM Standards, Amidi, Hajeck
1–30	103(a)	Spiers, Amidi
1–30	103(a)	Spiers, Amidi, Hajeck

III. ANALYSIS OF CHALLENGED GROUNDS

We now consider Petitioner's asserted grounds of unpatentability and Patent Owner's arguments to determine whether Petitioner has demonstrated by a preponderance of the evidence that the challenged claims would have been obvious under 35 U.S.C. § 103. *See* 35 U.S.C. § 316(e) (petitioner has the burden of proving unpatentability by a preponderance of the evidence).

A. Principles of Law

A claim is unpatentable under 35 U.S.C. § 103(a) if "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

A patent claim "is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR*, 550 U.S. at 418. An obviousness determination based on the teachings of multiple references requires finding "both 'that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.'" *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) (citation

omitted); *see also KSR*, 550 U.S. at 418. Further, an assertion of obviousness "cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at 418; *In re NuVasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (a finding of a motivation to combine "must be supported by a 'reasoned explanation'").

B. Level of Ordinary Skill in the Art

Factors pertinent to a determination of the level of ordinary skill in the art include "(1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field." *Envtl. Designs, Ltd. v. Union Oil Co. of Cal.*, 713 F.2d 693, 696 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.*, 707 F.2d 1376, 1381–82 (Fed. Cir. 1983)). "Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case." *Id.* at 696–697. The prior art may reflect an appropriate level of skill. *Okajima v. Bourdeau*, 261 F.3d 1350, 1354–55 (Fed. Cir. 2001).

Petitioner asserts a person of ordinary skill in the art "would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field." Pet. 8–9 (citing Ex. 1003 ¶ 67). Petitioner contends that additional training can substitute for educational or research experience, and vice versa. *Id.* at 8. Petitioner asserts that such a hypothetical person would have been familiar with the JEDEC industry

standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with a memory controller and other parts of a computer system, including standard communication busses and protocols, such as PCI and SMBus busses and protocols. *Id.* at 8–9. Petitioner further contends that such "a hypothetical person would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers." *Id.* at 9. Petitioner further asserts that such "a hypothetical person would further have been familiar with voltage supply requirements of such structures (e.g., memory modules, memory devices, memory controller, and associated access and control circuitry), including voltage conversion and voltage regulation circuitry." *Id.*

Patent Owner indicates "[f]or the purposes of this [Response], Patent Owner is applying the level of ordinary skill in the art proposed by Petitioner" for this proceeding. Resp. 1.

The evidence that Petitioner presents mostly applies to the educational level and experience of workers in the field, but also touches upon other factors as well, including problems and solutions in the prior art and complexity of the technology. *See* Pet. 7–8. We find Petitioner's proposal is consistent with the level of ordinary skill in the art reflected by the '918 patent and the prior art of record, and, therefore, we adopt Petitioner's proposed level of ordinary skill in the art, with the exception of the open-ended language "at least" which introduces ambiguity and may encompass skill levels beyond ordinary. *See Okajima v. Bourdeau*, 261 F.3d 1350,

1355 (Fed. Cir. 2001) (the prior art may reflect an appropriate level of skill in the art).

C. Claim Construction

We construe claim terms "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b) (2021). There is a presumption that claim terms are given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art in the context of the specification. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Nonetheless, if the specification "reveal[s] a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess[,] . . . the inventor's lexicography governs." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) (en banc) (citing *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002)). "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing Phillips, 415 F.3d at 1312–17). Only disputed claim terms must be construed, and then only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Matal*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

1. "Memory Module"

Patent Owner contends as follows:

> The term "memory module" appears in the preamble of the independent claims, which provides antecedent basis for the same term in the body of the text. The preamble is thus limiting

> as the District Court found after reviewing the specification in detail. The Court further explained that "a skilled artisan would understand a 'memory module' is distinct from, and has essential structural requirements not necessarily found in, other modular computer accessories. That includes the structure necessary to connect to a memory controller.

Resp. 1–2 (citing Ex. 2032, 28; Ex. 2034, 319). Patent Owner argues that the "court's ruling is consistent with the specification which states in the Overview section that the invention is particularly 'couplable to a *memory controller* of a host system.'" *Id.* at 2 (citing Ex. 1001, 1:66–67, 3:66–67). Patent Owner states that Petitioner "objected to the court's finding that the memory module is limiting, but does not dispute the Court'[s] finding on what a 'memory module' means to a [person of ordinary skill in the art]." *Id.* (citing Ex. 2033, 4).

As support for its argument, Patent Owner relies on a claim construction order issued by the District Court for the Eastern District of Texas, which states as follows:

> Having reviewed the entire patent "to gain an understanding of what the inventors actually invented and intended to encompass by the claim[s]," *Catalina Mktg. Int'l*, 289 F.3d at 808–09, the Court finds the preamble limiting. While the claims recite many of the structural requirements of a "memory module," the claims arguably read on other modular computer devices, such as a video card or network controller, despite no evidence the inventors intended to encompass such devices by the claims. To the contrary, as the Overview section [of the Court's claim construction order] explains, the invention "is couplable *to a memory controller* of a host system," [Ex. 1001] at 3:66–67 (emphasis added), not just the host system as recited in the claims. *See also id.* at 1:66–67 ("[t]he present disclosure relates generally to computer memory devices"). Thus, a skilled artisan would understand a "memory module" is distinct from,

> and has essential structural requirements not necessarily found in, other modular computer accessories. That includes the structure necessary to connect to a memory controller. *See Memory Systems: Cache, DRAM, Disk*, Dkt. No. 76-17 at 319 (depicting, in FIG. 7.6, a memory controller connected to two memory modules). Accordingly, the preambles are limiting.

Ex. 2032, 28) (alterations in original), *cited in* Resp. 2.

Patent Owner argues that Petitioner's expert, Dr. Wolfe, testified that the term "memory modules" typically refers to "main memory modules," which "are *designed to connect to the primary memory controller* for the purpose of holding general purpose code and data in a computer system." *Id.* at 2 (citing Ex. 2030, 123:14–25; Ex. 2056, 100:15–101:8 (by 2004–2005, a memory module "was intended to go into a dedicated memory slot and not a general-purpose IO slot")). Patent Owner contends that the '918 patent's usage of "memory module" is consistent with that understanding, and asserts that we should adopt the District Court's claim construction, including that the claimed "memory module" includes structures necessary to connect to a memory controller. *Id.* at 2–3 (citing Ex. 2031 ¶¶ 51–53); *accord* Sur-Reply 1.

In Reply, Petitioner contends that we properly found that Harris, the FBDIMM Standards, Amidi, and Spiers all disclose a "memory module" in our Institution Decision. Reply 1–2 (citing Inst. Dec. 14–15, 17–18, 34–37, 45; Pet. 19–20, 82–83; Reply 23–26). Petitioner contends that the District Court's construction did not limit "memory module" to only "***main*** memory modules . . . designed to connect to the ***primary*** memory controller." *Id.* at 1–2 (emphasis in original) (citing Resp. 2; Ex. 2032, 26–28, 35; Ex. 2030, 125:12–127:13; Ex. 2056, 100:15–101:19).

In Sur-Reply, Patent Owner disagrees with Petitioner's contention that "memory module" is not limited to "***main memory*** modules . . . designed to connect to the primary memory controller." Sur-Reply 1 (emphasis in original) (citing Reply 1). Patent Owner argues that Petitioner's contention "ignores the District Court's finding based on intrinsic evidence—which [Petitioner] did not object to—that the 'invention [i.e., the claimed memory module] 'is couplable *to a memory controller* of a host system,' [Ex. 1001] at 3:66–67 …, not just the host system as recited in the claims."' *Id.* (citing Ex. 2032, 28; Ex. 1001, 4:5–12, 4:14–24, 4:35–39, 4:45–51, 5:4–20, 4:36–50, 6:4–6, 6:25–29, 6:61–66, 7:1–4, 7:21–25, 7:29–34, 7:43–49, 7:54–57, 21:24–25, 22:53–58, 23:19–22, 26:43–51, 23:41–44).

The District Court's Claim Construction Order (Ex. 2032) issued after our Institution Decision (Paper 10). Although Petitioner argued in the District Court litigation that the claim preambles were not limiting, Petitioner does not appear to maintain that argument here following the District Court's determination that the preambles were limiting. Ex. 2032, 28. Since the term is recited in both the preambles and bodies of these claims, there is evidence that the inventors of the '918 patent intended the term to limit the claim, as the District Court determined. *See Catalina Mktg. Int'l., Inc. v. Coolsavings,com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002) (citing *Bell Commc'ns Rsch., Inc. v. Vitalink Communications Corp.*, 55 F.3d 615, 620 (Fed.Cir.1995) ("dependence on a particular disputed preamble phrase for antecedent basis may limit claim scope because it indicates a reliance on both the preamble and claim body to define the claimed invention.")).

We agree with Petitioner's contention that "memory module" is not limited to "*main* memory modules . . . designed to connect to the *primary* memory controller." Reply 1. The '918 patent states

> **In certain embodiments**, the device contains a high density Flash memory with a low density DRAM, wherein the DRAM is used as a data buffer for read/write operation. The Flash serves as the **main memory**.

Ex. 1001, 11:3–6 (emphases added). This is the only mention of "main memory" in the '918 patent. That the Flash memory serves as "main memory" in "certain embodiments" implies that there may be other embodiments in which this is not the case. Accordingly, we agree with Petitioner that the term "memory module" is not limited to "*main* memory modules . . . designed to connect to the *primary* memory controller." *See* Reply 1.

We agree with Patent Owner that the "memory module" includes structure to connect with a "host system" including its memory controller. *See, e.g.*, Ex. 1001, code (57), 12:52–59. The claims do not mention a "memory controller" but they do mention that the "memory module" has an "interface" to connect with a "host system." Ex. 1001, 38:19–24 (claim 1), 39:54–59 (claim 16), 40:51–56 (claim 23). That the "memory module" has structure for connecting to the host system's memory controller may thus be implied from the claims.

We agree with Petitioner that the District Court's determination was that the preambles of all claims of the '918 patent are limiting. Ex. 2032, 35. To the extent that the District Court's determination construed "memory module" to include structure necessary to connect to a memory controller, our construction of "memory module" is consistent.

2. "Pre-Regulated Input Voltage"

Claims 16–22 recite a "pre-regulated input voltage." Ex. 1001, 39:61, 42:23. Petitioner identifies at least two meanings for this claim term, one meaning within pre-determined limits and the other meaning the voltage must be pre-regulated on the memory board itself. Pet. 73. Petitioner contends that the District Court construed "pre-regulated input voltage" to have its plain and ordinary meaning, and rejected Samsung's argument that the voltage must be pre-regulated on the memory module. Reply 20, n.3 (citing Ex. 2032, 21–22, 34; Inst. Dec. 37–38; Ex. 2030, 268:18–270:5). Petitioner contends that Patent Owner's expert does not dispute the District Court's construction. *Id.* (citing Ex. 1075, 142:10–144:18). According to Petitioner, both experts agree that the V12V input to Harris can be pre-regulated under that construction. Reply 20 (citing *id.* at 5, n.2).

Patent Owner argues that a "pre-regulated input voltage is just a regulated voltage provided to these voltage conversion circuits." Resp. 38.

Under its ordinary and plain meaning in the context of the '918 patent, we understand "pre-regulated input voltage" to mean that the voltage is regulated before conversion to a stepped up or down level by the voltage converters. *See* Ex. 1001, code (57), 28:53–58, Fig. 16 (1110, 1112). This is consistent with Patent Owner's proposed construction.

D. Ground 1: Obviousness Over Harris and FBDIMM Standards

Petitioner contends claims 1–3, 8, 14, 15, and 23 would have been obvious over the combination of Harris and FBDIMM Standards and relies on the Declaration of Dr. Andrew Wolfe (Ex. 1003) in support. Pet. 14–51. For the reasons that follow, we are persuaded that the evidence, including

Dr. Wolfe's testimony, supports Petitioner's showing and establishes by a preponderance of the evidence that these claims are unpatentable.

1. Harris (Ex. 1023)

Harris is titled "Voltage Distribution System and Method for a Memory Assembly." Ex. 1023, code (54). Harris was published as U.S. Patent Pub. No. 2006/0174140 A1 on August 3, 2006. Petitioner contends Harris is prior art under § 102(a). Pet. 10.

Harris's Figure 1A is reproduced below.

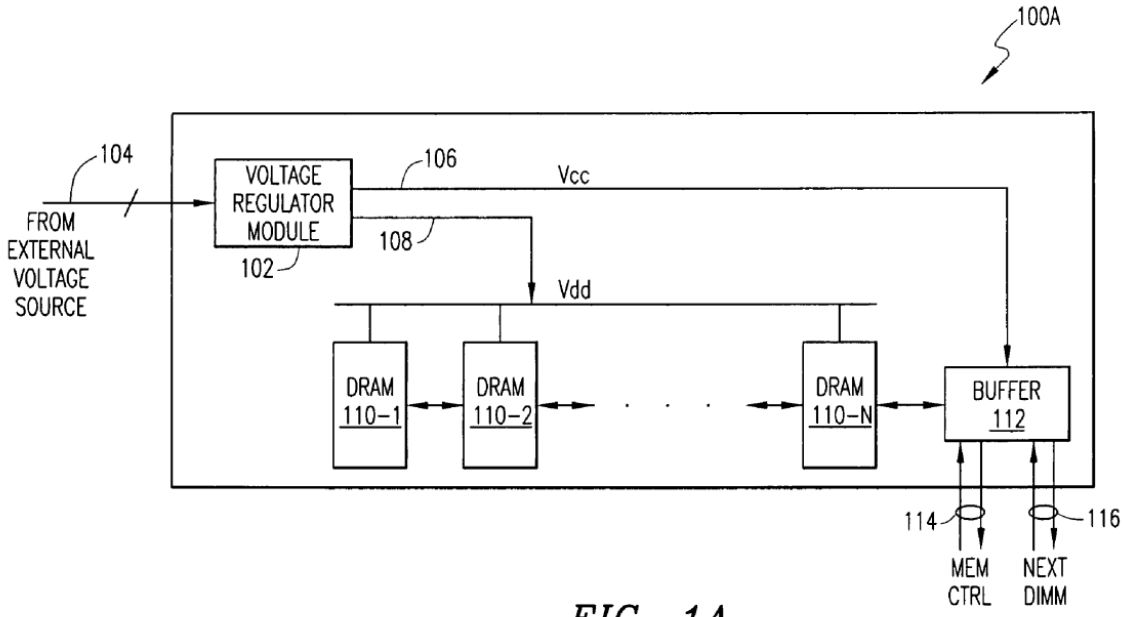


FIG. 1A

As shown in Figure 1A, Harris discloses a memory module 100A including on-board regulator 102 for converting an externally supplied voltage 104 to appropriate local voltage levels 106 (V_{cc}), 108 (V_{dd}), such as 0.5V to 3.5V. Ex. 1023, code (57), ¶¶ 9–10. Voltage 106 is supplied to buffer/logic component 112 which may be connected to a memory controller via interface 114 and daisy-chained with other memory assemblies via interface

116. *Id.* ¶ 9. Voltage 108 powers memory devices 110-1 to 110-N. *Id.* The memory module 100A may be a Dual In-Line Memory Modules (DIMM) wherein each of the memory devices 100-1 to 100-N comprises a Double Data Rate (DDR), DDR2, or DDR3 device. *Id.* The memory module 100A may be an unbuffered, registered or fully buffered DIMM. *Id.*

2. FBDIMM Standards (Exs. 1027, 1028)

In March 2007, the Joint Electron Device Engineering Council (JEDEC) published standards for Fully Buffered DIMM (FBDIMM) memory modules titled "JESD82-20" (Ex. 1027) and "JESD205" (Ex. 1028). Ex. 1029; Ex. 1003 ¶¶ 134–136. Petitioner refers to these standards collectively as the "FBDIMM Standards." Pet. 11. Petitioner contends the FBDIMM Standards are prior art under § 102(a). *Id.*

The FBDIMM Standards specify voltages for components on the memory module as follows:

Product Family Attributes

DIMM organization	x72 ECC			
DIMM dimensions (nominal)	30.35mm (height) x 133.35mm (width) x 8.2 mm (max thickness) MO-256 variation AB 30.35mm (height) x 133.35mm (width) x 8.8 mm (max thickness) MO-256 variation BB			
Pin count	240			
SDRAMs supported	256Mb, 512Mb, 1Gb, 2Gb, 4Gb			
Capacity	256MB, 512MB, 1GB, 2GB, 4GB, 8GB, 16GB			
Serial PD	Consistent with JC 45			
Supply voltages (nominal)	min	typ	max	
	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply
	3.0	3.3	3.6	(V_{DDSPD})
Buffer Interface	High-speed Differential Point-to-point Link at 1.5 volt			
DRAM Interface	SSTL_18			

Note 1: Approximate DC values, refer to AMB Component Specification for actual DC and AC values and conditions.
Note 2: Vtt range accomodates measurable offset due to complementary CA bus current paths. (See Vtt section)
An Unloaded system should supply Vtt of 0.48*Vdd/0.52*Vdd to Dimm socket

Ex. 1028, 9. The above table shows values for supply voltages including DRAM V_{DD}, AMB V_{CC}, DRAM interface V_{TT}, and V_{DDSPD}. The FBDIMMM Standards further specify the following voltages for various power supplies:

Table 9.2 — Pin Description (Sheet 3 of 3)

Signal	Type	Description
$\overline{\text{RESET}}$		Power Good Reset
Miscellaneous Test		
TEST (4 pins)	NC	Pin for debug and test. Must be floated on DIMM.
TESTLO (5 pins)	A	Pin for debug and test. Must be tied to Ground on DIMM
TESTLO_AB20	A	Pin for debug and test. Connected to two resistors. One resistor is connected to VCCFBD, the other resistor is connected to VSS.
TESTLO_AC20	A	Pin for debug and test. Connected to two resistors. One resistor is connected to VCCFBD, the other resistor is connected to VSS.
Power Supplies		
VCC (24 pins)	A	1.5V nominal supply for core IO
VCCFBD (8 pins)	A	1.5V nominal supply for FBD high speed IO
VDD (24 pins)	A	1.8V nominal supply for DDR IO
VSS (156 pins)	A	Ground
VDDSPD	A	3.3V nominal supply for SMB receivers and ESD diodes
Other Pins		
BFUNC	I	**Buffer Function Bit:** When BFUNC = 0, AMB is used as a regular buffer on FB-DIMM. When BFUNC = 1, AMB is used as either a repeater or a buffer for LAI function. On FB-DIMM, BFUNC is tied to Ground
RFU (18 pins)	NC	**Reserved for Future Use.** Must be floated on DIMM. RFU pins denoted by "a" are reserved for forwarded clocks in future AMB implementations.
Other No Connect Pins		
NC (129 pins)	NC	No Connect pins

Ex. 1027, 83. The table above sets voltage levels for power supplies V_{CC}, V_{CCFBD}, V_{DD}, V_{SS}, and V_{DDSPD}.

3. Motivation to Combine

Petitioner contends that a person of ordinary skill in the art would have been motivated to combine Harris with the FBDIMM Standards with a reasonable expectation of success because Harris states that its Figure 1A may be a "fully buffered DIMM" (FBDIMM or FBD). Pet. 16 (citing Ex. 1023 ¶¶ 9–13; Ex. 1003 ¶¶ 158–165). Petitioner contends that a person of ordinary skill in the art would have understood that this type of DIMM is standardized in JEDEC's FBDIMM Standards and thus would naturally look to them for more details about the "fully buffered DIMM" that Harris

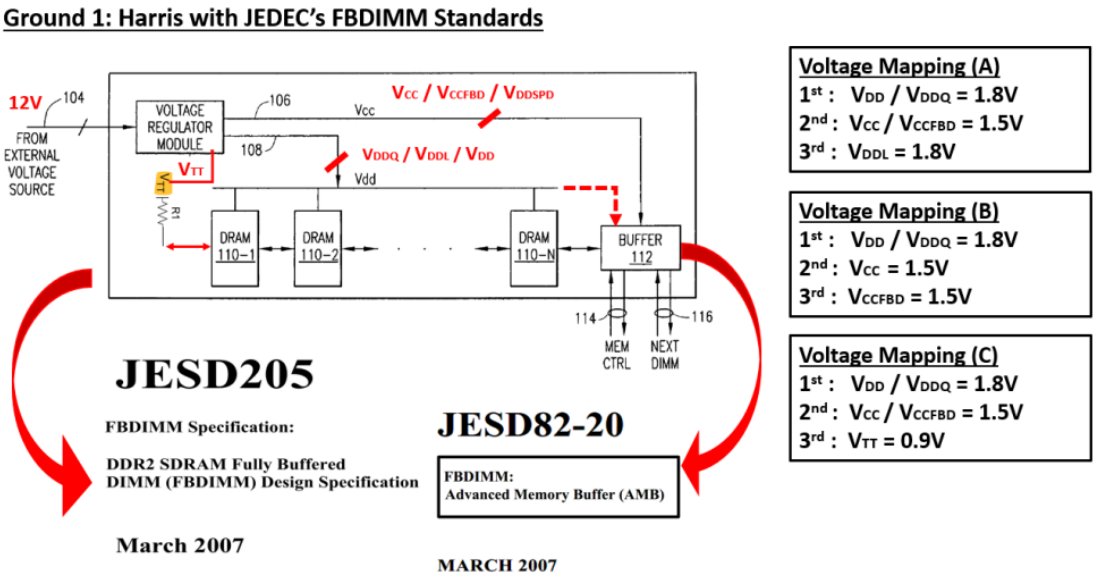
describes as compatible with his on-board voltage regulator module (VRM). *Id.*

To explain its combination, Petitioner provides the following table:

	Voltage Mappings (Grounds 1-3)		
	A	B	C
"*first*":	V_{DD} or V_{DDQ} = 1.8V	V_{DD}, V_{DDQ}, or V_{DDL} = 1.8V	V_{DD}, V_{DDQ}, or V_{DDL} = 1.8V
"*second*":	V_{CC} or V_{CCFBD} = 1.5V	V_{CC}=1.5V	V_{CC} or V_{CCFBD} = 1.5V
"*third*":	V_{DDL}=1.8V	V_{CCFBD}=1.5V	V_{TT}=0.9V
"*fourth*":	V_{DDSPD}=3.3V	V_{DDSPD}=3.3V	V_{DDSPD}=3.3V

Pet. 27. The table above shows Petitioner's Voltage Mappings A, B, and C from the FBDIMM Standards for Grounds 1–3, and how they disclose the "first," "second," "third," and "fourth regulated voltages" in the claims. *Id.*

For Ground 1, Petitioner provides the illustration below:



Pet. 15. This illustration shows how Petitioner is combining the teachings of Harris and the FBDIMM Standards to arrive at the claims. Specifically,

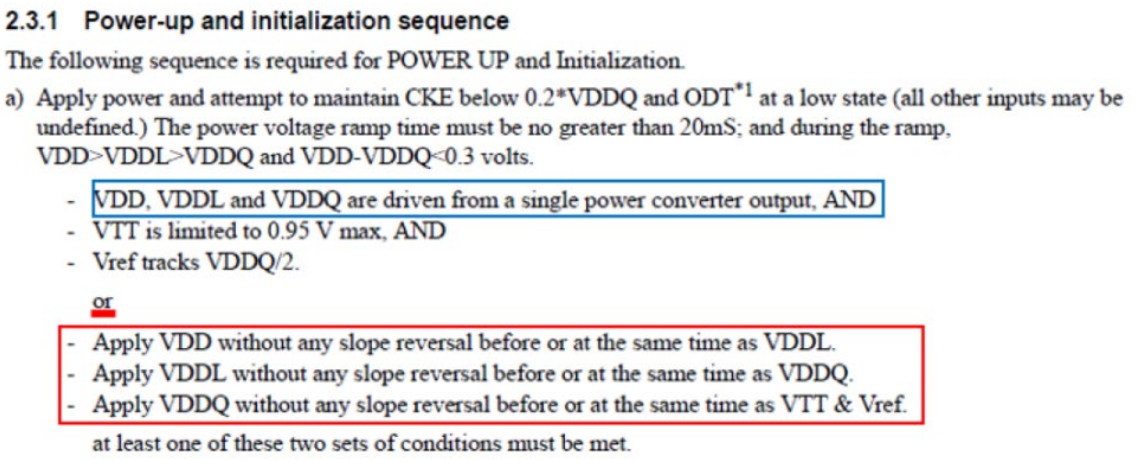
JEDEC FBDIMM Standard JESD205 applies to Harris's memory module and JESD82-20 applies to the Harris's buffer.

a) Modifying Harris to Have Four Converters

Patent Owner asserts that a person of ordinary skill in the art would not have modified Harris's memory module to have four converters, as Petitioner asserts. Resp. 17–21. Patent Owner argues that Harris discloses a single converter providing at least two voltages in each of Petitioner's voltage mappings. *Id.* at 17 (citing Ex. 2031 ¶¶ 75–79). Patent Owner asserts that Harris discloses "***a*** high-frequency switching voltage converter capable of generating tightly-controlled voltage level**s**." (Emphases original) *Id.* (citing Ex. 1023 ¶ 10, Fig. 1A); *see also* Sur-Reply 15–17.

Petitioner replies that the Petition explained the motivation for multiple converters, including that "the JEDEC standards treat those voltages separately, thus permitting power-on sequencing; providing independent control; improving efficiency; and saving power." Reply 14 (citing Pet. 30–31; Ex. 2030, 39:2–10, 44:25–46:10; Ex. 1075, 134:22–136:2, 194:23–195:7; Ex. 1062, 13–15). In addition, Dr. Wolfe explains that smaller, lower-power regulators may be more desirable than larger, higher-power regulators because they can be less costly. Ex. 2030, 45:21–25. He also stated that space availability on the memory board can require separate regulators. *Id.* at 46:1–4. In sum, Dr. Wolfe stated that "a number of ordinary engineering factors" would be considered when deciding to use one supply for both voltages or two separate supplies. *Id.* at 46:5–10.

Petitioner provides the following excerpt from the JEDEC standards to explain its position:



2.3.1 Power-up and initialization sequence

The following sequence is required for POWER UP and Initialization.

a) Apply power and attempt to maintain CKE below 0.2*VDDQ and ODT*1 at a low state (all other inputs may be undefined.) The power voltage ramp time must be no greater than 20mS; and during the ramp, VDD>VDDL>VDDQ and VDD-VDDQ<0.3 volts.

- VDD, VDDL and VDDQ are driven from a single power converter output, AND
- VTT is limited to 0.95 V max, AND
- Vref tracks VDDQ/2.

or

- Apply VDD without any slope reversal before or at the same time as VDDL.
- Apply VDDL without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.

at least one of these two sets of conditions must be met.

Reply 14 (citing Resp. 25; Ex. 1026, 9 (DDR2); Ex. 1046, 15 (same for DDR3); Pet. 30–31. The excerpt from JEDEC's JESD79-2B (DDR2) and JESD79-3A (DDR3)[2] above shows two options for compliance with these standards, one shown partially with a blue box,[3] the other with a red box. Although the first option (blue box) indicates that a single converter generates the voltages, Petitioner correctly contends that the second option (red box) does not list that any converter provides these voltages, but leaves open how they are generated. *Id.* at 13–14. A person of ordinary skill in the

[2] Although Petitioner does not expressly rely on JEDEC's JESD79-2B (DDR2) and JESD79-3A (DDR3) in its combinations, the parties seem to be in agreement that these specifications are part of the background knowledge that a person of ordinary skill in the art would have had. In an obviousness analysis, the background knowledge is properly considered together with the demands known in the design community, and the inferences and creative steps that a person of ordinary skill in the art would employ. *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362 (Fed. Cir. 2013).

[3] In our opinion, Petitioner should have drawn the blue box to include the following two lines "VTT is limited to 0.95 V max, AND Vref tracks VDDQ/2" because of the way the standard presents the two sets of conditions with the word "or" between them and refers to them as "two sets of conditions." We refer to the two sets of conditions as "options" herein.

art would have understood that the listed voltages may be generated with respective converters. *See* Ex. 1026, 9; Ex. 1046, 15; Ex. 1003 ¶ 242 (Dr. Wolfe testifying that JESD79-2B's disclosure that the voltage supplies can be turned on and off separately suggests to a person of ordinary skill in the art that the voltages are provided by separate converters); *see also KSR*, 550 U.S. at 418 ("a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.").

Moreover, Harris discloses "***at least one*** on-board voltage regulator module (VRM) is provided as part of the memory board assembly module 100A for converting externally supplied voltage level available on external source path 104 into appropriate local voltage levels that power the first and second voltage paths, i.e., the V_{dd} and V_{cc}." Ex. 1023 ¶ 10 (emphases added). Also, Harris's claim 1 recites "***at least one*** voltage regulator module for converting an externally supplied voltage level into appropriate ***voltage levels*** that power said first and second voltage paths, respectively." Ex. 1023, claim 1. Thus, Harris discloses that multiple converters can be used to generate respective multiple voltage levels.

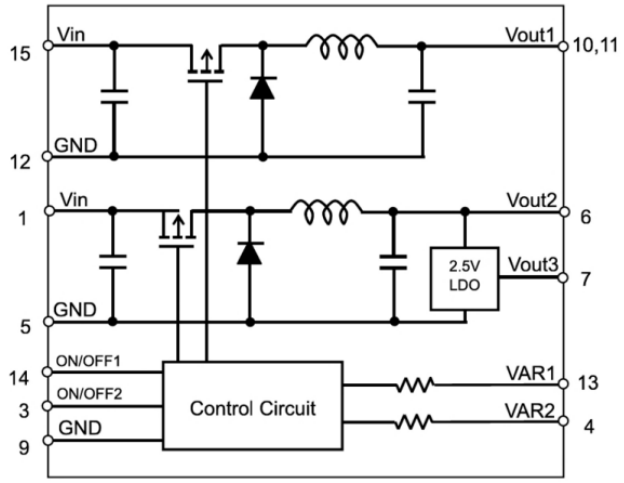
Furthermore, Petitioner contends that Patent Owner's examples relate to a SODIMM, not an FBDIMM like Harris. Reply 14 (citing Resp. 23; Ex. 2006, 4 ("SODIMM"); Ex. 1075, 102:17–103:9 (SODIMM is unbuffered as shown in Ex. 2045 and Ex. 2046, 4.20.11-23)). Although Harris discloses unbuffered DIMMs may be an option to use, Petitioner relies upon Harris's FBDIMM teachings in its Petition. *See, e.g.*, Pet. 16, Ex. 1023 ¶ 9, claim 24.

Patent Owner further argues that single buck converters with multiple voltage outputs were known in the art. Resp. 18 (citing Ex. 2031 ¶ 80;

Ex. 2003; Ex. 2004). As Petitioner shows, however, single buck converters for generating single voltages were also known in the art. Pet. 91 (citing Ex. 1023, Fig. 6 (640)); Ex. 1047, 1:28–32, 2:47–55, 5:56–59, 7:6–14; Ex. 1041, 1–2, 9; Ex. 1042, 16; Ex. 1048, 1–2; Ex. 1058, 5). Although Patent Owner is correct that Petitioner must show a reason for using separate buck converters, as already explained, Petitioner did so. Reply 15 (sequencing the power, turning power on and off independently, saving cost, eliminating cross-coupling of noise, and solving space constraints); Ex. 2030, 45:21–46:10 (smaller regulators may be less costly than larger ones, and may be desirable when separate spaces are available on the memory board). Thus, we do not agree with Patent Owner's argument that Petitioner "has not articulated any advantage of using one converter per voltage if Harris already uses a single converter for at least two voltages." Sur-Reply 11 (citing Reply 11–14; Ex. 1023 ¶ 10).

We also find Patent Owner's distinction between a single converter generating two voltages and two separate converters is not meaningful because of how the single converter may be internally constructed. For example, Petitioner presents the following illustration:

DC-DC Converter Specification(DRAFT)
MPD4S014S



Reply 13 (citing Ex. 1075, 127:21–129:24, 228:25–232:19; Ex. 1042, 16 (corresponding to EX1048, 2)). The figure above shows two buck converters receiving two Vin inputs and generating respective outputs Vout1 and Vout2 (the LDO Vout3 can be disregarded in this discussion). Externally, this chip resembles a single converter, and has effectively only one input if the pins 1 and 15 are tied together, but internally it has two buck converters generating respective voltages. Thus, the presence of multiple outputs suggests, to a person of ordinary skill in the art, that multiple buck converters are being used or, at least, that such a configuration is a suitable option.

Patent Owner next argues that a tightly spaced FBDIMM does not allow for the large inductors that multiple buck converters would require, and a person of ordinary skill in the art would not have modified Harris to add more components. Resp. 18–21 (citing Ex. 2031 ¶¶ 83–84; Ex. 2101, 20 (illustration of FBDIMM prototype); Ex. 2042, 7 (illustration of FBDIMM)).

Patent Owner also argues that one could use a single-inductor four-output buck converter instead of separate ones. *Id.* at 20–21.

Petitioner counters that defining the number of converters based on the number of inductors lacks any support in the '918 patent. Reply 12 (citing Ex. 1001; Ex. 2032). Petitioner argues that "it was well known that a single chip can include multiple buck converters (and inductors)." *Id.* (citing Ex. 1048, 1–2; Ex. 1075, 106:24–109:8 (discussing use of inductor in buck converter); Ex. 2030, 98:8–18 (same); Ex. 1058, 5, 14–15 (similar)). Petitioner also contends that space for multiple buck converters is not mentioned in the '918 patent or its claims, since solving any such problem was within the level of ordinary skill in the art. Reply 13 (citing *id.* at 19–20; Ex. 2030, 53:16–54:14, 89:1–21).

Petitioner has shown that one of ordinary skill in the art would have implemented a memory module with four buck converters to generate respective voltages in at least some situations. Patent Owner may be right that four buck converters using a single inductor would have been the more typical or preferred approach, as Dr. Mangione-Smith implied. *See, e.g.*, Ex. 2031 ¶¶ 76, 81–84. However, "it is not necessary to show that a combination of prior art references is the best option, only that it be a suitable option." *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023); *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021); *PAR Pharm., Inc. v TWI Pharms., Inc.*, 773 F.3d 1186, 1197–98 (Fed. Cir. 2014).

b) Use of Separate Converters to Generate $V_{DD}/V_{DDQ}/V_{DDL}$ or V_{CC}/V_{CCFBD}

Patent Owner argues against Petitioner's showing of a motivation to combine by arguing that neither Harris nor the FBDIMM Standards suggest separate power rails for V_{DD}/V_{DDQ} and V_{DDL} or V_{CC} and V_{CCFBD} for Voltage Mappings A and B. Resp. 21–30. Patent Owner argues that the DDR2 Specification that Petitioner cited requires that the voltages V_{DD}, V_{DDQ} and V_{DDL} are driven from a single power converter output. *Id.* at 22 (citing Ex. 1026, 9; Ex. 2061 ¶ 87). As discussed previously, Patent Owner argues that the DDR2 Specification requires a single converter (see text in blue box of Exhibit 1026, 9 above) whereas Petitioner relies on the second option (see text in red box) which does not specify how the voltages are to be generated. Although Patent Owner's argument is correct for the first option, it is not for the second option, which is the one on which Petitioner relies.

Patent Owner argues that Dr. Wolfe concedes that in all standard FBDIMMs that he was aware of, V_{DDL}, V_{DD} and V_{DDQ} for the DRAMs are connected to a single power converter, and are not individually powered on or off. Resp. 22–23 (citing Ex. 2030, 133:5–134:6, 39:11–40:24). Dr. Wolfe stated "I'm not aware of any [FBDIMMs with three different power rails] on the market. Obviously, the teaching is right here in the JEDEC specification." Ex. 2030, 133:10–17. We understand Dr. Wolfe to be referring to the second option boxed in red in the above excerpt from JEDEC's JESD79-2B (DDR2) (Ex. 1026) and JESD79-3A (DDR3) (Ex. 1046), on which Petitioner relies. Patent Owner argues that Petitioner is suggesting a design that persons of ordinary skill in the art were aware of, but rejected, and that this is evidence of non-obviousness. Resp. 22–23.

We do not agree that a person of ordinary skill in the art would have rejected the design, however, when the JEDEC specification allows for it and Harris discloses that it is an option for generating V_{CC} and V_{DD}. Ex. 1026, 9; Ex. 1023 ¶ 9. Extending Harris's teaching to generate four voltages with respective voltage regulators is within the level of ordinary skill in the art. *See* Ex. 2030, 43:10–14 (Dr. Wolfe stating four voltages specified by JEDEC would require use of four power supplies in most situations); 160:2–3 ("it would be obvious to use four power supplies"); Ex. 1003 ¶¶ 146–149 (credible testimony showing that buck converters were well known to persons of ordinary skill in the art). "A person of ordinary skill is also a person of ordinary creativity, not an automaton." *KSR*, 550 U.S. at 421.

Patent Owner argues that a single power converter was required so that the voltages track one another during power up. Resp. 23–24 (citing Ex. 2006, 4; Ex. 2061 ¶ 88; Ex. 1023 ¶ 12). But Dr. Wolfe indicates that the voltages of separate converters can be made to track one another by coupling their feedback, which was a known option. Ex. 2030, 54:25–55:13. Patent Owner does not refute Dr. Wolfe's testimony.

Patent Owner argues that JEDEC's JESD79-2B (DDR2) and JESD79-3A (DDR3) do not address power generation on the memory module, only the inputs and outputs of the memory device. Resp. 24–25. Petitioner replies that Harris teaches a module that supplies all the voltages needed on the module, which would include all those needed by the memory devices. Reply 14–15 (citing Ex. 2030, 37:13–38:5); *see also* Ex. 1023 ¶ 9. Patent Owner's argument views these JEDEC specifications, which would have been general knowledge of one of ordinary skill in the art, in isolation

without considering them together in the combination of Harris and the FBDIMM Standards. *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362 (Fed. Cir. 2013) ("[T]he Court required an analysis that reads the prior art in context, taking account of 'demands known to the design community,' '***the background knowledge possessed by a person having ordinary skill in the art***,' and 'the inferences and creative steps that a person of ordinary skill in the art would employ.'" (emphasis added)); *In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986) (citing *In re Keller*, 642 F.2d 413, 425 (CCPA 1981) ("Non-obviousness cannot be established by attacking references individually where the rejection is based upon the teachings of a combination of references.").

Patent Owner asserts that Petitioner's contention that an FBDIMM has separate pins for V_{DD}, V_{DDQ} and V_{DDL} does not support its contention of separate converters, "particularly where it was known that there are stability and timing benefits when using a single source." Resp. 24 (citing Ex. 2006, 4). Dr. Wolfe explains that the FBDIMM module of Petitioner's combination would not have separate pins to receive V_{DD}, V_{DDQ} and V_{DDL} but would derive them onboard the module from the 12-volt input pin. Ex. 2030, 35:25–36:15. As to stability, Dr. Wolfe testifies that a feedback loop maintains stability in light of current variations, temperature changes, and other factors. *Id.* at 64:25–65:10. As to timing, Dr. Wolfe indicated that separate converters can track one another by coupling their feedback, and that this was a known option. *Id.* at 54:25–55:13.

Patent Owner further argues that sequencing the different voltages does not require separate converters. Resp. 24–27. Petitioner contends that this was the obvious way to implement the JEDEC specifications (boxed in

red above) with several benefits. Reply 15 (citing Ex. 1003 ¶ 256). We agree with Petitioner that separate converters were an option that one of ordinary skill in the art would have used in some practical circumstances for reasons of cost, space availability, etc.

Patent Owner argues that it was actual practice for persons of ordinary skill in the art to use a single power converter to generate the necessary voltages. Resp. 25 (citing Ex. 2030, 133:5–134:6, 39:11–40:24). Although using a single power converter may have been the most common approach, this does not negate Petitioner's showing that a person of ordinary skill in the art would have considered separate converters desirable under certain circumstances. *See Elekta Ltd. v. ZAP Surgical Systems, Inc.*, 81 F.4th 1368 (Fed. Cir. 2023) (quoting *Novartis Pharms. Corp. v. West-Ward Pharms. Int'l Ltd.*, 923 F.3d 1051, 1059 (Fed. Cir. 2019) ("Nor does an obviousness showing 'require that a particular combination must be the preferred, or the most desirable, combination described in the prior art in order to provide motivation . . . .'").

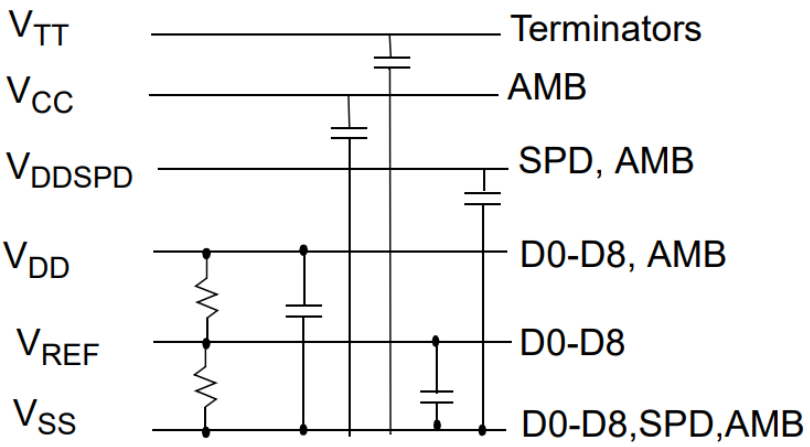
Patent Owner similarly argues that V_{CC} and V_{CCFBD} are separate voltages with separate pins, but asserts that Petitioner does not explain why a single on-board V_{CC} power source is insufficient for V_{CC} and V_{CCFBD} power rails when a single set of V_{CC} interface pins providing power from the host met the power needs for both V_{CC} and V_{CCFBD}. Resp. 25–27 (citing Pet. 30–31; Ex. 1028, 11–12; Ex. 2031 ¶ 92). For similar reasons as explained for V_{DD}, V_{DDQ} and V_{DDL}, we disagree. As Petitioner indicates, using separate converters for V_{CC} and V_{CCFBD} provides the benefits of sequencing the power, turning power on and off independently, saving cost, eliminating cross-coupling of noise, and solving space constraints. Reply 15

(citing Ex. 2060, 39:2–10, 44:25–46:10; Ex. 1075, 134:22–136:2, 194:23–195:7; Ex. 1062, 13–15; Ex. 2012, 73; Ex. 1003 ¶ 255).

Patent Owner's arguments do not undercut Petitioner's showing of a motivation to combine.

c) Use of Third Buck Converter for V_{TT}

Patent Owner contends that Petitioner's Voltage Mapping C relies on three different voltages, including a termination voltage, V_{TT}, connected to terminators. Resp. 27 (citing Pet. 26, 30; Ex. 1028, 13, 15–16). For context, the relevant figure from the JEDEC JESD205 specification is reproduced below:

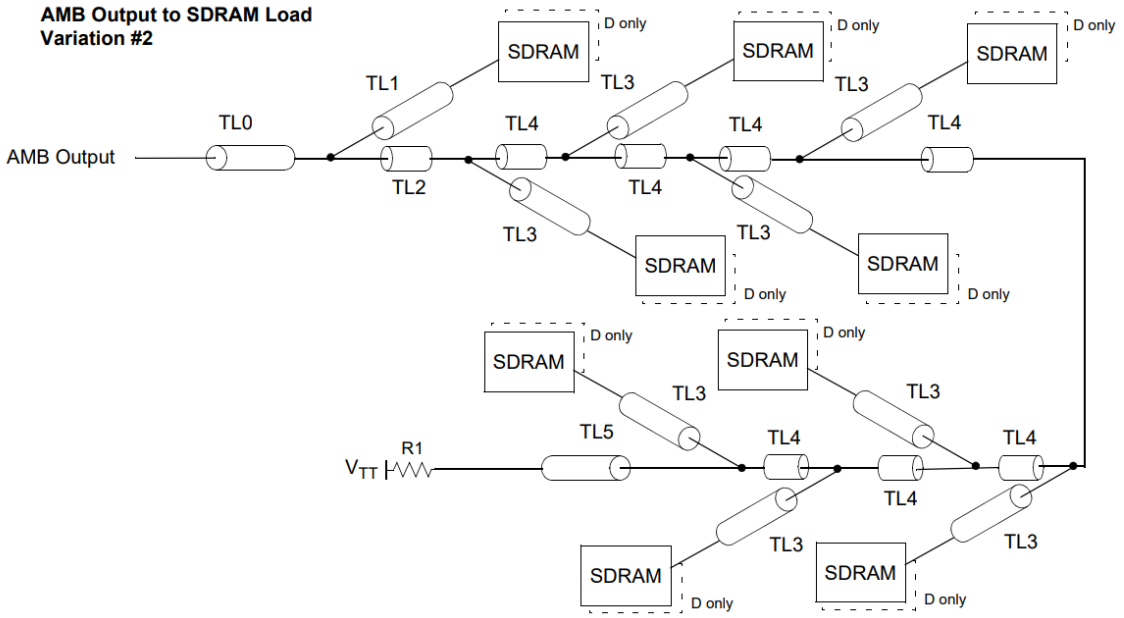


Ex. 1028, 13. The above figure shows various voltages V_{TT}, V_{CC}, V_{DDSPD}, V_{DD}, V_{REF}, V_{SS} and their relationship to one another according to the JEDEC JESD205 specification. *Id.*

Patent Owner argues that Harris does not disclose generating V_{TT} on its module and argues that it would be supplied from the motherboard instead because this would ensure that all DIMMs have the same termination voltages and eliminate ground loops that could degrade signal integrity. Resp. 27–28 (citing Ex. 2061 ¶ 96); Sur-Reply 17–18. Patent Owner further argues that design complexity favors having a single regulator for a group of

DIMMs rather than one regulator per DIMM. Resp. 28–29 (citing Ex. 1027, 20; Ex. 2031 ¶ 97; Ex. 2012, 72). In addition, Patent Owner argues that Petitioner touted JEDEC's move of voltage regulation from the motherboard to the DIMM as a "major design improvement" and Patent Owner asks, "If it had been so obvious, why did it take the industry so long to make that design improvement?" *Id.* at 29. Patent Owner further argues that generating V_{TT} is not one of two choices, and that V_{TT} is generally not provided to DDR2 modules; passive termination is used instead. *Id.* at 33 (citing Ex. 2061 ¶ 98; Ex. 2044, 6; Ex. 2045, 6; Ex. 2046, 4.20.11-6; Ex. 2006, 5).

In Reply, Petitioner contends that Harris teaches generating all of the voltages on the module, including all of the voltages for an FBDIMM, which would include V_{TT}. Reply 15 (citing Inst. Dec. 20–23; Ex. 1023 ¶ 12; Ex. 2030, 30:15–20, 72:22–73:7, 103:11–104:23, 109:5–111:10, 239:8–20). Petitioner contends that "Harris's module provides the voltages for the buffer 112 to send address and control signals to the DDR memory devices, which the FBDIMM Standards make clear require not just V_{DD}, but also V_{TT} to terminate those signals." *Id.* (underlining omitted) (citing Pet. 17–18; Ex. 1028, 9, 15, 68). Petitioner reproduces the figure below:



Reply 16 (reproducing the figure at Ex. 1028, 68). The above figure is from the FBDIMM Standards and shows the net structure routing for addresses and commands from the advanced memory buffer (AMB) to the SDRAMs and how they are terminated by V_{TT}. *Id.* Petitioner contends that V_{TT} is required by the JEDEC Standards to track V_{DD} (Ex. 1028, 15) which is why dual buck converters for generating V_{DD} and V_{TT} were readily available. Reply 16–17 (citing Ex. 1028, 9; Ex. 2030, 72:22–73:7, 196:3–197:7; Ex. 1040, 1, 11; Ex. 1041, 1; Ex. 1048).

We agree with Petitioner that the combination of Harris and the FBDIMM Standards at least suggests that V_{TT} can be generated onboard the memory module. Reply 15–17 (citing Pet. 17–18; Inst. Dec. 20–24; Ex. 1023 ¶ 12; Ex. 1028, 9, 15, 68; Ex. 1040, 1, 11; Ex. 1041, 1–2, 7–9; Ex. 1048; Ex. 1075, 112:12–114:8; Ex. 2030, 30:15–20, 57:17–20, 58:18–59:10, 72:22–73:7, 103:11–104:23, 109:5–111:10, 140:15–24, 196:3–197:7, 239:8–20). Harris indicates that its on-board voltage regulator converts externally supplied voltage into appropriate local voltage levels for powering

memory devices of the memory assembly module. Ex. 1023, code (57), ¶¶ 12, 16, Fig. 2, step 204. Petitioner shows that V_{TT} is needed onboard a memory module to terminate address and control signals. Reply 15 (citing Pet. 17–18; Ex. 1028, 9, 15, 68). In addition, Petitioner shows that V_{TT} is required by JEDEC to track V_{DD}, which is why dual buck converters for generating these voltages were commercially available. Reply 16–17 (citing Ex. 1028, 9; Ex. 2030, 72:22–73:7, 196:3–197:7; Ex. 1040; Ex. 1041, Ex. 1048). In light of these facts and the teachings of Harris and the FBDIMM Standards, Petitioner has shown that a person of ordinary skill in the art would have added to the memory module a third buck converter to generate V_{TT}.

Patent Owner further argues that "even if V_{TT} is generated on module, there is no reason that it should be generated by a buck converter." Resp. 29. Patent Owner contends that, "[a]s Micron noted, . . . an LDO would be sufficient to power V_{TT}." *Id.* (citing Ex. 2006, 7; Ex. 2007–2010; Ex. 2050). Patent Owner contends that an LDO is much smaller than a buck converter, which requires a controller and discrete components such as an inductor, which makes the LDO preferable given the space constraint. *Id.* (citing Ex. 2061 ¶ 99). Patent Owner also argues that an LDO is preferred when the current load is below 1A. *Id.* at 29–30 (citing Ex. 2031 ¶ 99; Ex. 2047, 21; Ex. 2048, 23; Ex. 2049, 20; Ex. 1040, 23–24, Figs. 22–25).

In Reply, Petitioner contends that buck converters were commercially available for V_{TT} and provided high efficiency compared to an LDO. Reply 17 (citing Ex. 1075, 112:12–114:8 (LDO may be only 10% efficient); Ex. 2030, 57:17–20, 58:18–59:10 (buck converters up to 98% efficient), 140:15–24 (trend has been to use buck converters). We agree with

Petitioner that, under some circumstances, one of ordinary skill in the art would have chosen a buck converter over an LDO for the reasons that Petitioner mentions.

d) Use of Buck Converter to Provide V_{DDSPD}

Patent Owner argues that Petitioner's voltage mappings A–C all relate the recited "fourth regulated voltage" to the 3.3V V_{DDSPD}. Resp. 30 (citing Pet. 26). Patent Owner contends that Harris's reasons for on-module regulation do not apply to V_{DDSPD}. *Id.* Specifically, Patent Owner argues that the "3.3V-supply voltage is sufficiently high such that a regulator on the motherboard could readily provide the needed 300mV tolerance; and the same SPD [serial presence detect] can be used for different generations of DRAMs." *Id.* (citing Ex. 2031 ¶ 102); *see also* Sur-Reply 18–19.

Petitioner replies that Harris teaches generating all of the voltage onboard the module, including all of the voltages for an FBDIMM, which would include V_{DDSPD}. Reply 18 (citing Ex. 1023 ¶ 12; Pet. 16–18). Petitioner further contends there are only two options—generating the voltages on the motherboard or on the module—rendering either option obvious. *Id.* (citing Inst. Dec. 24).

We agree with Petitioner that Harris teaches generating voltages onboard the memory module, which suggests this would include V_{DDSPD} as it is one of the voltages required in the FBDIMM standards. Ex. 1023 ¶¶ 9–12; Ex. 1028, 15. As Petitioner contends, Harris teaches generating the voltages required in the FBDIMM standards on the memory module, and the FBDIMM standards set out what those voltages are. Ex. 1023 ¶¶ 9–12; Ex. 1028, 15.

We also agree with Petitioner that there are only two options: either V_{DDSPD} is generated on the motherboard or on the module, rendering either option obvious. Reply 18. "[W]hen there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *KSR*, 550 U.S. at 421.

Patent Owner argues, if V_{DDSPD}'s are supplied both on the motherboard and individual DIMMs, they cannot track one another, which would lead to communication problems when they are at different voltage potentials. Resp. 30–31 (citing Ex. 2031 ¶ 102). Patent Owner also argues that "3.3V is a common power rail on the motherboard such that it can be supplied to FBDIMMs without the increased cost and problems associated with providing a regulator for each of Harris' modified FBDIMM memory boards." *Id.* at 31 (citing Ex. 2031 ¶ 102; Ex. 2038, 13 (3.3V PSU output)).

As previously discussed, Dr. Wolfe indicated that separate converters can track one another by coupling their feedback. Ex. 2030, 54:25–55:13. We recognize, however, that this may require connection and coordination across the motherboard-DIMM interface.

Harris mentions in its background a voltage supply level of 3.3V, which is the nominal value for V_{DDSPD} in the JEDEC standards. Ex. 1028, 9. Harris also states that it is one of the values that "keeps getting lower" with each generation of DIMM/DRAM technology, implying that it should be generated not on the motherboard, but on the FBDIMM. Ex. 1023 ¶ 2. One of ordinary skill in the art thus would have recognized that V_{DDSPD} may be generated onboard the memory module when considering Harris's teachings. Ex. 1023 ¶¶ 9–12.

We also note that the JEDEC FBDIMM standards provide that V_{DDSPD} can vary within the range of 3.3V +/- 0.3 V. Ex. 1029, 9. As long as the voltage is maintained within this range on both the motherboard and the FBDIMM, the implementation is compliant with the JEDEC standards.

Patent Owner further argues that, for the low currents required for components using V_{DDSPD}, buck converters would have been highly inefficient. Resp. 31 (citing Ex. 2051, D-1(up to 5mA active power supply current); Ex. 2052, 6, Table III (I2C power consumption less than 15mW on average; and @3.3V, current is less than 5mA); Ex. 1040, Figs. 22–25 (efficiency less than 20% at 10mA current); Ex. 2031 ¶ 103 (an LDO with a 12V-input-3.3V-output would be 26% efficient); Ex. 1062, 14 (using LDO to generate 3.3V from 12V)). Patent Owner asserts that a person of ordinary skill in the art would have used LDOs to generate V_{DDSPD}. *Id.*

Petitioner replies that Patent Owner concedes that the claimed "converter circuit" can be an LDO (Resp. 30, n.5). Reply 18. Petitioner also contends that "using a buck converter . . . was an obvious, highly efficient, and clearly 'suitable' option for converting 12V to 3.3V for V_{DDSPD} . . . regardless of whether [Patent Owner] considers it 'inferior' to an LDO." Reply 18 (citing Ex. 1048, 2; Ex. 1003 ¶¶ 146–49, 286; Ex. 2030, 76:4–19, 78:18–79:7, 79:24–80:11, 82:7–85:10, 88:4–20, 89:1–21, 138:14–21, 140:15–24; *Dome Pat. L.P. v. Lee*, 799 F.3d 1372, 1381 (Fed. Cir. 2016).

From the foregoing discussion, it is apparent that there are advantages and disadvantages to generating V_{DDSPD} onboard the memory module. However, "simultaneous advantages and disadvantages ... do[ ] not necessarily obviate motivation to combine." *Qualcomm*, 21 F.4th 784 (Fed. Cir. 2021) (citing *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed.

Cir. 2006)). Petitioner has shown that the advantages outweigh the disadvantages in at least some scenarios that the person of ordinary skill in the art would have considered desirable to pursue. Petitioner has shown that a person of ordinary skill in the art would have had reasons to combine Harris and the FBDIMM Standards with a reasonable expectation of success.

e) Conclusion on Motivation to Combine Harris and the FBDIMM Standards

On this record, Petitioner has shown by a preponderance of the evidence that a person of ordinary skill in the art would have combined Harris and the FBDIMM standards since Harris states that its memory module may include fully buffered DIMMs (FBDs). Ex. 1023 ¶ 9. We agree that one of ordinary skill in the art would have recognized Harris's mention of FBDIMMs as a standard and looked to the FBDIMM Standards for information concerning the voltage values standardized for use in an FBDIMM. Ex. 1027, 83; Ex. 1028, 9. For these reasons and others set forth above, we determine that one of ordinary skill in the art would have combined Harris and the FBDIMM Standards with a reasonable expectation of success.

4. Analysis of Independent Claim 1

a) Limitation 1.a: "A memory module comprising:"

Petitioner asserts that Harris's memory module 100A in Figure 1A or memory module 306-1 in Figure 3 corresponds to the claimed "memory module." Pet. 19–20 (citing Ex. 1023 ¶¶ 9, 17, 20, Figs. 1A, 3; Ex., 1003 ¶¶ 216–222; Ex. 1028, 38). Harris does indeed disclose a memory module with multiple memory devices such as DRAMs 110-1 to 110-N in Figure 1A or 306-1, for example, in Figure 3.

Patent Owner does not dispute that the preamble is met by Harris. *See* Resp.

Based on our review and consideration of the record, we determine that Petitioner has shown that Harris teaches the preamble.

> *b) Limitation 1.b: "a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system"*

Petitioner asserts that Harris and the FBDIMM Standards disclose this limitation. Pet. 20–25. Petitioner contends that Harris and the FBDIMM Standards disclose printed circuit boards (PCBs). Pet. 20–21 (citing Ex. 1023 ¶¶ 13, Figs. 1A, 3). Petitioner also contends that a PCB may be referred to as a "memory board" or "raw card." *Id.* at 20–21 (citing Ex. 1023 ¶ 9, Ex. 1028, 10, 38, 84; Ex. 1003 ¶¶ 223–225).

As for the PCB "*having an interface configured to fit into a corresponding slot connector of a host system*," Petitioner notes that Harris's Figure 3 shows that each memory module 306-1 to 306-M includes an edge connection for fitting into a corresponding slot of a host system. Pet. 21 (citing Ex. 1023 ¶¶ 2, 12, 13, 19, Figs. 3, 4; Ex. 1028, 38, 84; Ex. 1003 ¶¶ 226–227).

Petitioner further contends that Harris, consistent with the FBDIMM Standards, discloses that the edge connections are "*configured to couple power, data, address and control signals between the memory module and the host system*." Pet. 21–25. Petitioner contends that the power signal corresponds to Harris's voltage 104 in Figure 1A. *Id.* at 21 (citing Ex. 1023 ¶¶ 10, 12, 19). Petitioner contends that Harris's buffer 112 in Figure 1A is

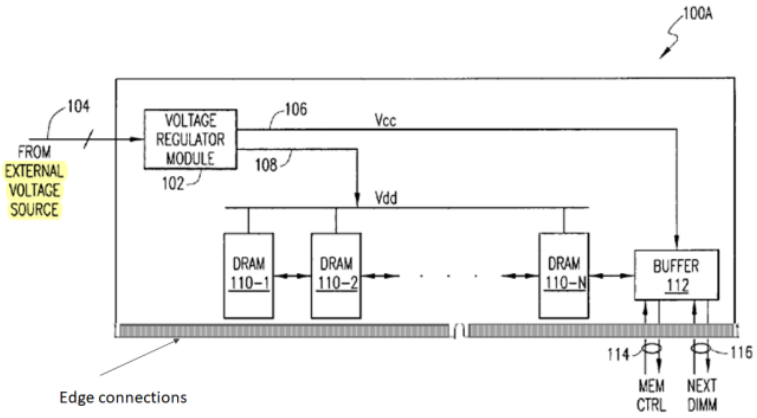
called "AMB" (Advanced Memory Buffer) in the FBDIMM Standards. Pet. 22–23. Petitioner indicates that Harris's buffer 112 receives data, address, and control signals via memory controller interface 114 and transmits these signals to DRAMs 110-1 to 110-N in Figure 1A. Pet. 22 (citing Ex. 1023 ¶ 9 ("buffer/logic component 112 is provided for buffering *command/address* (C/A) space as well as *data* space at least for a portion of memory devices 110-1 through 110-N"). In addition, Petitioner argues that the FBDIMM Standards indicate that buffer AMB receives data signals DQ0–DQ63; address signals A0–A15; and control signals RAS, CAS, WE, CS, etc. Pet. 22–23 (citing Ex. 1028, 13).

(1) Power from the Interface with the Host System

Patent Owner argues that all challenged claims require a memory module that includes a printed circuit board (PCB) having an interface with edge connections configured to couple power between the memory module and the host system. Resp. 3. According to Patent Owner, Harris does not disclose such a memory module. *Id.* Instead, Patent Owner asserts, Harris replaces the power supply interface pins with as few as six +12V non-interface pins from an external power source which is unregulated and has a wide tolerance, which does not comport with the regulated sources associated with a host system. *Id.* at 4, 6, 7 (citing Ex. 1023 ¶¶ 12, 16; Ex. 2030, 62:21–25, 63:1–8, 92:9–95:8; Ex. 2031 ¶¶ 60–66; Ex. 2037, 22; Ex. 2038, 13, Table 2); *see also* Sur-Reply 2–6. Patent Owner further argues that Harris supposedly provides a "technology-independent voltage distribution scheme for memory devices wherein system board power supply and associated voltage plane(s) are eliminated." Resp. 4 (citing Ex. 1023

¶ 19). Patent Owner argues that Harris effectively decouples the host system's voltage supply from the memory module. *Id.* at 5 (citing Ex. 2031 ¶ 38).

To illustrate its points, Patent Owner provides the following annotated figure:



Resp. 5. In the figure above, Patent Owner has modified Harris's Figure 1A to show edge connections along the bottom edge of memory board 100A, and highlights that the external voltage is connected to the side of the memory board. Patent Owner asserts that external sources connected to the side or top of a memory module were known. *Id.* at 5 (citing Ex. 2035; Ex. 2036, 41–42; Ex. 2031 ¶ 59).

In addition, Patent Owner argues that Petitioner's expert, Dr. Wolfe, testified that, in computer systems using FBDIMMs, the power supply units provide regulated voltages. *Id.* at 6 (citing Ex. 2030, EX2030, 62:21–25, 63:1–8, 92:9–95:8; Ex. 2037, 22, Table 15; Ex. 2038, 13, Table 2). According to Patent Owner, it would be "inadvisable" to provide unregulated voltages via a memory board to a memory slot because the "unregulated voltages could cause random noise patterns and degrade signal integrity." *Id.* at 7 (citing Ex. 2031 ¶¶ 65–66). Even with regulated voltage

sources, Patent Owner asserts, the voltage was not supplied via the DIMM interface. *Id.* (citing Ex. 2031 ¶ 66). Patent Owner argues that Petitioner's modified FBDIMM is powered from an external power source "wherein system board power supply and associated voltage plane(s) are eliminated." Resp. 8 (citing Ex. 1023 ¶¶ 10, 12, 19). Patent Owner further argues that neither Dr. Wolfe nor Dr. Mangione-Smith was aware of any memory controllers that supplied power supply voltages to DIMMs, and that Patent Owner did not provide evidence that a person of ordinary skill in the art would have known how to design a memory controller that supplied power to DIMMs. *Id.* at 8–9 (citing Ex. 1023 ¶ 17; Ex. 2030, 130:19–131:10; Ex. 2031 ¶ 67).

Although Patent Owner acknowledges that Harris discloses that its external voltage sources can be any "known or heretofore unknown voltage supplies, either regulated or unregulated," Patent Owner argues that this would sweep in the type of voltage supply that Harris seeks to eliminate. *Id.* at 9 (citing Ex. 2031 ¶ 68). Patent Owner further asserts that "nothing suggests that the voltage paths are via the memory slot to the interface edge connections." *Id.* at 9–10 (citing Ex. 2031 ¶ 69). Furthermore, Patent Owner asserts that different edge pins would be needed for different voltage sources independently distributed through the motherboard, increasing, rather than decreasing, the cost for power distribution in the motherboard and pin count on the DIMM connector to the motherboard. *Id.* at 10 (citing Ex. 1023 ¶¶ 13, 19–20; Ex. 2031 ¶ 70). Patent Owner summarizes its argument, stating that Harris teaches to eliminate power distribution to the DIMM slot, a feature which Petitioner does not propose to modify. *Id.* at 10–11; *see also* Sur-Reply 6. Patent Owner argues that Harris does not

couple power between the module and the host system, and therefore does not disclose elements 1.b, 16.b, 23.b and 16.f. *See* Pet. xi (1.b), xiii (16.b), xiv (16.d), and xvii (23.b). Patent Owner argues that the specific benefits Harris teaches can be achieved by decoupling power between the motherboard and memory module. Resp. 11 (citing Ex. 1023 ¶¶ 19, 20; Ex. 2031 ¶¶ 26, 58, 70). Patent Owner argues that the same arguments apply to claim 13. *Id.*

Petitioner replies that Patent Owner does not dispute that the FBDIMM Standards teach supplying power via edge connection, and that Patent Owner's expert, Dr. Mangione-Smith, admits that such edge connections were "standard." Reply 2 (citing Pet. 16–21; Resp. 3–11; Inst Dec. 18–20; Ex. 1075, 97:16–98:18, 163:16–20; Ex. 1077, 9). Petitioner also contends that Harris's reference to externally supplied voltage requires power external to the entire host system, but Harris merely requires power external to the DIMM memory module. *Id.* (citing Pet. 21–22; Resp. 3–11; Ex. 2030, 66:7–19, 67:20–68:21, 91:22–92:7, 129:24–130:17).

Petitioner further replies that Patent Owner wrongly modifies Harris's Figure 1A (above) to suggest that Harris would never use edge connections at the bottom for power. Reply 3. To illustrate its points, Petitioner reproduces the following annotated figure:

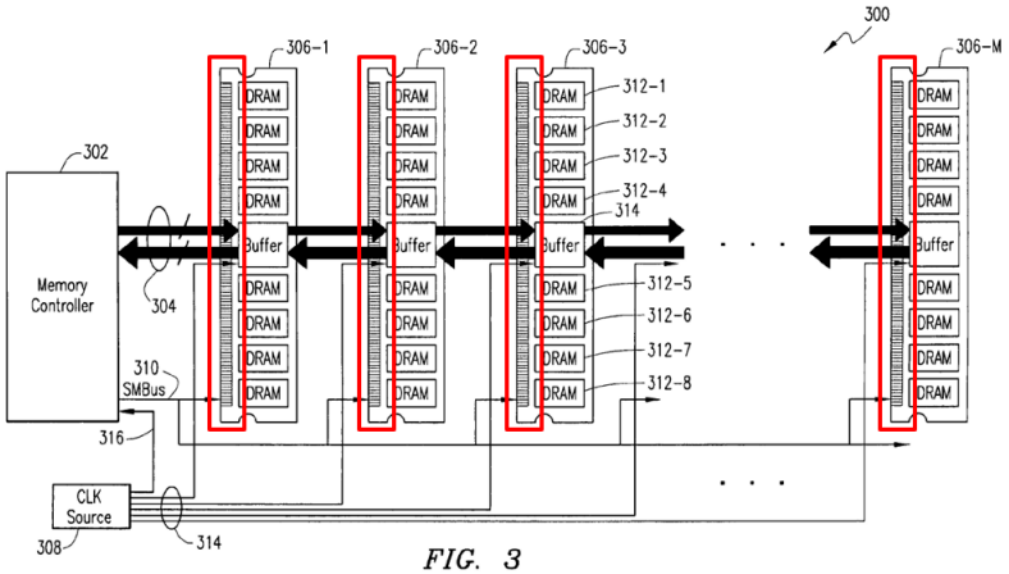


FIG. 3

Reply 4 (citing Ex. 1023, Fig. 3). In Harris's Figure 3 as annotated by Petitioner, above, Petitioner shows that Harris's memory modules 306-1 to 306–M are connected to the memory controller only through edge connections (boxed in red), meaning that power must come from those edge connections. *Id.* at 3–4. Petitioner further asserts that Harris's Figure 3 is nearly identical to an Intel drawing where the memory modules admittedly receive power through the edge connections form the host system. *Id.* at 4 (citing Ex. 1075, 171:4–17; Ex. 2101, 4). According to Petitioner, Harris confirms that, "[a]lthough not explicitly shown in this FIGURE [3, above], each memory board also receives a supply voltage …[which] may be sourced from the memory controller 302 [which is part of the host system, Ex. 1075, 167:23–168:1] or from a separate voltage source." *Id.* (quoting Ex. 1023 ¶ 17) (alterations in original). Petitioner's expert, Dr. Wolfe, explained that it was common for the host to supply power through edge connectors "alongside the memory controller signals." *Id.* (quoting Ex. 2030, 131:3–5).

Petitioner contends that Patent Owner misinterprets Harris to conclude that the system power supply is eliminated entirely. *Id.* at 4–5 (citing Ex. 1023 ¶ 19; Resp. 4–5, 8, 10–11). To the contrary, Petitioner argues, Harris proposes avoiding the need for different system board voltages such as "3.3V, 2.5V, 1.8V, 1.5V and beyond," by simply supplying a single voltage (i.e., "12V") to the memory module so that an "on-board voltage regulator module [e.g., 102 above] [can] generate appropriate local voltage levels" on the memory module. *Id.* at 5 (citing Ex. 1023 ¶¶ 2, 3, 12–13, 19). Petitioner contends, as Dr. Wolfe explained, Harris's "technology-independent voltage distribution scheme" eliminates the need for a "system-board-specific power supply," not all power. *Id.* (citing Ex. 2030, 116:10–117:6).

Petitioner contends that using edge connectors like those shown in Harris's Figure 3 is consistent with Harris's use of the known FBDIMM design, except with "few[er]" power pins given the higher 12V input voltage. Reply 6 (citing Ex. 1023 ¶ 12; Ex. 2030, 100:12–101:19, 102:17–25, 103:11–104:23). Petitioner argues that to prevent "accidental damage" due to this change in the power pins of the edge connector, Harris teaches changing "the board's connector keyway" so that it is "not interchangeable with the standard DIMM." *Id.* (citing Ex. 1023 ¶ 13; Ex. 2030, 117:7–21). According to Petitioner, this was a standard technique for memory modules receiving power from the host via the edge connections. *Id.* (citing Ex. 2016, 6–7; Ex. 2101, 21–22; Ex. 1075, 171:21–175:20). Patent Owner disagrees, stating that the keyway connector does not mean the 12V pins are added to the edge connection. Sur-Reply 5.

Petitioner asserts that Patent Owner's argument that "[s]upplying power…from [the] side…was known" "misses the point: regardless of

whether a side connection was possible, that would not negate the obviousness of using edge connections for power, as was highly common." Reply 7 (citing *Dome Pat. L.P. v. Lee*, 799 F.3d 1372, 1381 (Fed. Cir. 2015) (existence of a better alternative "does not mean that an inferior combination is inapt for obviousness purposes"). Petitioner states that Patent Owner's "expert admitted that using ***both*** was a known option, consistent with the combination for Grounds 2 to 3." *Id.* (emphasis Petitioner's). According to Petitioner, the side connection could be used for battery backup, as taught by Amidi, and the edge connections could be used for power from the host system during normal operation, as taught by Harris. *Id.* (citing Ex. 2035, 39; Ex. 1075, 165:10–166:12).

Considering the foregoing, we determine that Petitioner has shown that the combination of Harris and the FBDIMM Standards discloses limitation 1.b (and claim 13). Harris states that DRAM devices may be "powered from system board or main board voltage sources." Ex. 1023 ¶ 2. Although this is presented in the background of Harris, and Patent Owner argues that it is technology over which Harris seeks to improve, it is nonetheless information that a person of ordinary skill in the art would have known. Harris's teaching of "replacing" power supply interface pins with as few as six +12V pins" means that those six pins take the place of the 72 pins in the interface, implying that power still comes from the interface with the host system. *Id.* ¶ 12. Harris reinforces this by disclosing that "the supply voltage may be sourced from the memory controller 302 or from a separate voltage source." *Id.* ¶ 17. Although Patent Owner argues that Dr. Wolfe nor Dr. Mangione-Smith could recall any DIMM memory module powered by a memory controller, Harris expressly discloses this feature. *Id.*

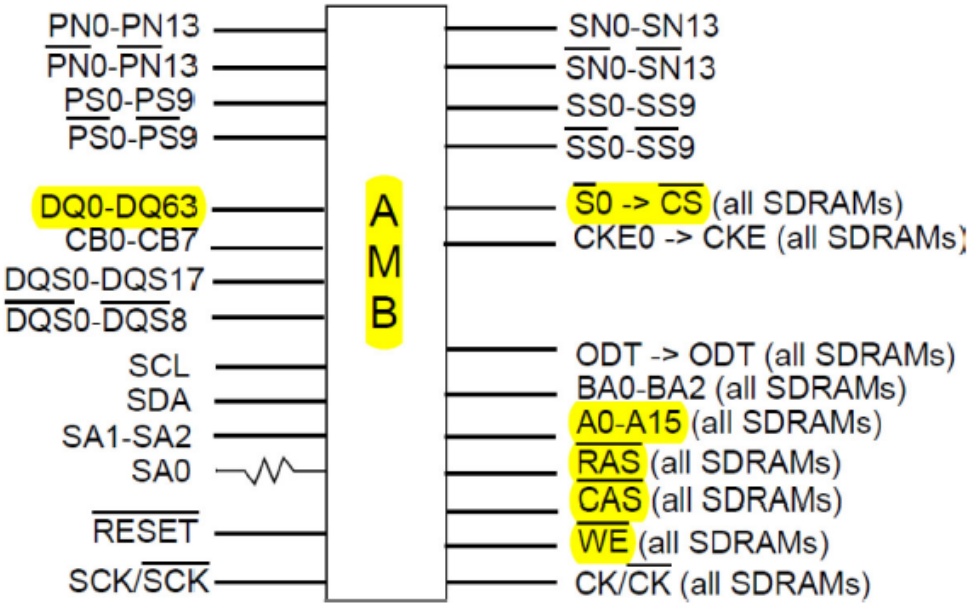
Harris further teaches that "external voltage sources may comprise any combination of known or heretofore unknown voltage supplies, either regulated or unregulated, and even including variable voltages." Ex. 1023 ¶ 14. This means there may be more than one voltage supply, either regulated or unregulated, as Petitioner contends (which may be the host system and a backup source, for example). Dr. Wolfe explains that Harris's statement that "system board power supply and associated voltage plane(s) are eliminated" means that "supplies such as the memory [V_{DD}] and the memory [V_{CC}] that are specific to a particular generation of memory chips . . . can be supplied on the DIMM rather than being supplied from the motherboard." Ex. 2030, 116:25–117:6.

Furthermore, Petitioner indicates that the FBDIMM Standards show that the buffer AMB may be connected to a host, suggesting that the FBDIMM derives its power from the host. Pet. 24 (citing Ex. 1027, 4). The experts agree that it was common at the time for the host system to provide the regulated 12V power supply to the FBDIMM, and commercially available devices are in evidence. Ex. 2030, 62:21–25, 63:1–8, 92:9–95:8; Ex. 2037, 22, Table 15, Ex. 2038, 13, Table 2; Ex. 2031 ¶ 65; Ex. 1075, 180:14–183:3; Ex. 2038, 8, 13. These facts point to the conclusion that the external voltage source may be the host system in the combination of Harris with the FBDIMM Standards notwithstanding Patent Owner's arguments to the contrary.

(2) Data, Address, and Control Signals Via Edge Connection

Claim 1 recites an "interface including a plurality of edge connections configured to couple … data, address and control signals between the

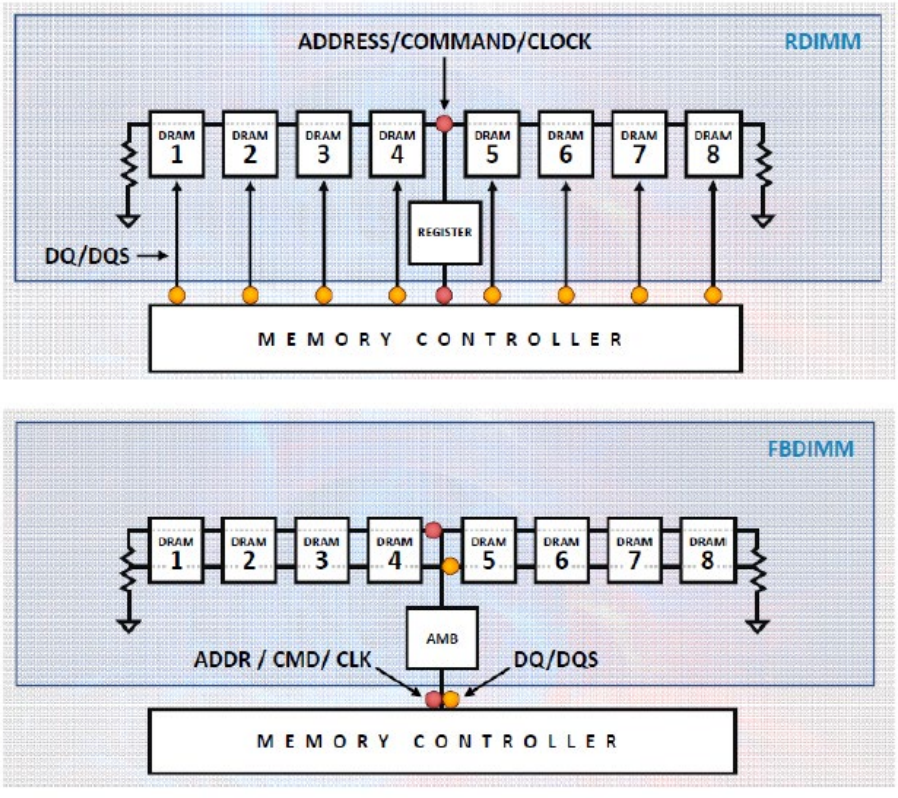
memory module and the host system." Ex. 1001, 38:23–25. Patent Owner argues that the DIMM and AMB do not receive data signals (DQ0–DQ63) or address and control signals (A0–A15, RAS, CAS, WE) from the host. Resp. 11 (citing Pet. 22–25). According to Patent Owner, these signals are instead generated by the AMB based on decoded FBDIMM channel signals (PS[9:0] and PS[9:0]bar). *Id.* at 11–12 (citing Ex. 2031 ¶ 72; Ex. 1027, 3–4; Ex. 1028, 29; Ex. 2039, 2; Ex. 2101, 4; Ex. 2040, 1). Patent Owner argues that Petitioner's evidence does not show that the data, address and control signals are received from the host. *Id.* at 15. Specifically, Patent Owner relies on the figure below from the FBDIMM Standards (*see* Sur-Reply 7 (citing Ex. 1028, 13)).



According to Patent Owner, the above figure shows that data, address and controls signals (highlighted in yellow) are generated and outputted by the buffer, and are not received from the DIMM interface. Sur-Reply 6–7 (citing Pet. 22–23; Resp. 11–15; Ex. 2031 ¶¶ 72–74). Patent Owner contends this does not comport with the claim language which requires an

"interface including a plurality of edge connections configured to couple … data, address and control signals between the memory module and the host system." *Id.* at 8 (citing Ex. 1001, 22:1–6). Patent Owner argues that Dr. Wolfe merely stated that the AMB outputs "information" to the DRAMs but the claims require specific "signals," not just "information." *Id.* at 8 (citing Ex. 1003 ¶ 230; Ex. 2030, 7:20–11:6). Patent Owner argues that the outputs from the AMB are not transmitted over FBDIMM's edge connections. *Id.*

Petitioner argues that Patent Owner's technology tutorial indicates that an FBDIMM receives address and control signals similar to an RDIMM, as shown below:



Reply 7–8 (citing Ex. 1077, 8–9; Ex. 1075, 91:23–92:19, 95:14–96:13, 97:16–98:18). The figures above show that the memory controllers transmit

address, command and clock signals (shown in red), or information containing these signals, to the register (RDIMM) or AMB (FBDIMM), which transmits them to the DRAMs. *Id.*; Sur-Reply 9.

Petitioner contends that the host system provides address, command and clock signals to the AMB encoded as a packetized, serialized signal on fewer wires than would be required to receive them as separate, parallel signals. Reply 8–9 (citing Resp. 11–12; Ex. 2031 ¶ 31; Ex. 1075, 155:22–157:1, 212:3–8, 213:3–215:20, 219:13–220:9, 226:7–228:8; Ex. 2030, 8:3–11:6). Petitioner alleges that Patent Owner is in essence attempting to rewrite the claims to require dedicated pins for these signals, which the claims do not require. *Id.* at 9.

Patent Owner argues that it is not attempting to rewrite the claims to require "dedicated pins" as Petitioner alleges. Sur-Reply 8–9 (citing Reply 8–9). Patent Owner asserts that the pin names indicate what "signals" are exchanged at the interface between the host and the FBDIMM, as shown in the figure below.

Pin Name	Pin Description	Count
	FB-DIMM Channel Signals	99
SCK	System Clock Input, positive line	1
$\overline{SCK}$	System Clock Input, negative line	1
PN[13:0]	Primary Northbound Data, positive lines	14
$\overline{PN}$[13:0]	Primary Northbound Data, negative lines	14
PS[9:0]	Primary Southbound Data, positive lines	10
$\overline{PS}$[9:0]	Primary Southbound Data, negative lines	10
SN[13:0]	Secondary Northbound Data, positive lines	14
$\overline{SN}$[13:0]	Secondary Northbound Data, negative lines	14
SS[9:0]	Secondary Southbound Data, positive lines	10
$\overline{SS}$[9:0]	Secondary Southbound Data, negative lines	10
FBDRES	To an external precision calibration resistor connected to Vcc	1
	DDR2 Interface Signals	175
DQS[8:0]	Data Strobes, positive lines	9
$\overline{DQS}$[8:0]	Data Strobes, negative lines	9
DQS[17:9]/DM[8:0]	Data Strobes (x4 DRAM only), positive lines. These signals are driven low to x8 DRAM on writes.	9
$\overline{DQS}$[17:9]	Data Strobes (x4 DRAM only), negative lines	9
DQ[63:0]	Data	64
CB[7:0]	Checkbits	8
A[15:0]A, A[15:0]B	Addresses. A10 is part of the pre-charge command	32
BA[2:0]A, BA[2:0]B	Bank Addresses	6
$\overline{RASA}$, $\overline{RASB}$	Part of command, with $\overline{CAS}$, $\overline{WE}$, and $\overline{CS}$[1:0].	2
$\overline{CASA}$, $\overline{CASB}$	Part of command, with $\overline{RAS}$, $\overline{WE}$, and $\overline{CS}$[1:0].	2
$\overline{WEA}$, $\overline{WEB}$	Part of command, with $\overline{RAS}$, $\overline{CAS}$, and $\overline{CS}$[1:0].	2
ODTA, ODTB	On-die Termination Enable	2
CKE[1:0]A, CKE[1:0]B	Clock Enable (one per rank)	4
$\overline{CS}$[1:0]A, $\overline{CS}$[1:0]B	Chip Select (one per rank)	4
CLK[3:0]	CLK[1:0] used on 9 and 18 device DIMMs. CLK[3:0] used on 36 device DIMMs. CLK[3:2] should be output disabled when not in use.	4
$\overline{CLK}$[3:0]	Negative lines for CLK[3:0]	4
DDRC_C14	DDR Compensation: Common return pin for DDRC_B18 and DDRC_C18.	1
DDRC_B18	DDR Compensation: Resistor connected to common return pin DDRC_C14	1
DDRC_C18	DDR Compensation: Resistor connected to common return pin DDRC_C14	1
DDRC_B12	DDR Compensation: Resistor connected to V_{SS}	1
DDRC_C12	DDR Compensation: Resistor connected to V_{DD}	1

Ex. 1028, 29. The figure above shows Patent Owner's highlighting to show the "FB-DIMM Channel Signals" including PS[9:0] and PS[9:0]bar, and the "DDR2 Interface Signals" including DQ0–DQ63, A0–A15, RAS, CAS, and WE. Patent Owner states that all memory control for the DRAM resides in the host, and argues that the fact that all read, write, and configuration accesses are addressed to the DIMM does not undermine that the signals Petitioner relies on are generated and outputted by the buffer, and not exchanged at the interface between the FBDIMM and the host. Sur-Reply 9 (citing Ex. 2030, 7:20–11:6; Ex. 2030 ¶ 230).[4]

[4] Patent Owner's citation to "Ex. 2030 ¶ 230" appears to be an error and we cannot determine from the context what Patent Owner intended to cite.

Petitioner further argues that the FBDIMM is a preferred embodiment in the '918 patent, and excluding a preferred embodiment from the claims is "rarely, if ever correct." Reply 9 (citing *Kaufman v. Microsoft Corp.*, 34 F.4th 1360, 1372 (Fed. Cir. 2022)). To the contrary, Patent Owner argues that the claims need not encompass FBDIMM embodiments, which are disclosed but unclaimed subject matter. Sur-Reply 10 (citing *Maxwell v. J. Baker, Inc.*, 86 F.3d 1098, 1107 (Fed. Cir. 1996); Ex. 1001, 21:38–55).

According to Petitioner, Patent Owner concedes that the signals (PS[9:0] and PS[9:0]bar) received by the AMB result in data, address, and control signals needed by DDR2 SDRAMS. Reply 9 (citing Ex. 2031 ¶ 31). Petitioner further notes that the FBDIMM Standards state that all memory control for the DRAM resides in the host, including memory request initiation, and that the AMB acts as a DRAM memory buffer for all read, write, and configuration accesses addressed to the DIMM. *Id.* (citing Ex. 1027, 1). As a buffer for all such commands to the FBDIMM, Petitioner asserts, the AMB must necessarily couple data, address, and control signals from the host system to the memory module as the claims require. *Id.*

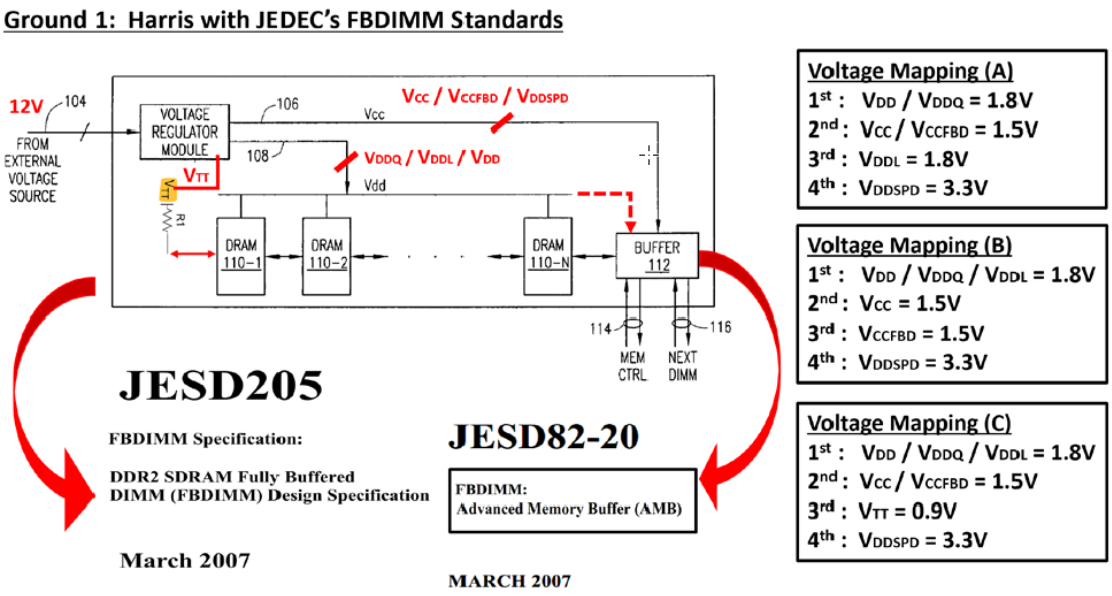
Petitioner and Patent Owner agree that FBDIMM AMB receives information that contains data, address, and control signals encoded in packetized, serialized form at its edge connections via the signals PS[9:0] and PS[9:0]bar, and that the AMB uses these signals to generate data, address and command signals including DQ0–DQ63, A0–A15, RAS, CAS, and WE provided to the DIMMs onboard the memory module. Pet. 21–23; Sur-Reply 10. The claims merely require an "interface including a plurality of edge connections configured to couple … data, address and control signals between the memory module and the host system." Ex. 1001, 38:23–

25. We determine that the data, address, and control signals of Harris and the FBDIMM Standards as received at edge connections coupling the memory module and host system satisfy this claim limitation, even though the signals are in encoded, packetized, or serialized form and thus may be received at the same pin or pins. That the signals are encoded, packetized, and serialized does not change the fact that they are data, address, and control signals. The claims do not require these signals to be received at the edge connections in any particular form or on any particular pins. *See In re Self*, 671 F.2d 1344, 1348 (CCPA 1982) (stating that limitations not appearing in the claims cannot be relied upon for patentability).

Based on our review and consideration of the record, we determine that Petitioner has shown that the combination of Harris and the FBDIMM Standards teaches this limitation.

> *c) Limitations 1.c to 1.f: "a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; a third buck converter configured to provide a third regulated voltage having a third voltage amplitude; a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude;"*

Petitioner contends that Harris and the FBDIMM Standards disclose limitations 1.c to 1.f. Pet. 26–31. Petitioner relies on an annotated version of Harris's Figure 1A, shown below.



Above is Harris's Figure 1A annotated with information one would have obtained from the FBDIMM Standards according to Petitioner. Pet. 26 (citing Pet. 14–19; Ex. 1003 ¶¶ 232–243, 250–257, 262–276, 281–287). Specifically, the above figure shows voltage mappings A, B, and C of four voltages specified by Harris and the FBDIMM Standards. Petitioner contends the voltage range described in Harris (0.5V–3.5V) is the same range as the voltages described in the FBDIMM Standards. *Id.* at 27 (citing Ex. 1023 ¶ 9). Petitioner contends the voltages would be "*regulated*" because Harris indicates "tightly *regulated* power" is a problem to be solved, and proposes "at least one *on-board* voltage *regulator*" that is "capable of generating tightly-controlled voltage levels" as the solution. *Id.* at 28 (citing Ex. 1023 ¶¶ 2, 3, 9–11; Ex. 1003 ¶ 234).

Petitioner further contends that Harris teaches using "buck converters" to provide the four regulated voltages. *Id.* (citing Ex. 1003 ¶¶ 236, 237, 252, 264, 286). Specifically, Petitioner contends that Harris discloses "replacing [the prior art] power supply interface pins with as few as six +12V pins

(from an external voltage source)" and then using "*a high-frequency switching voltage converter* capable of generating *tightly-controlled* voltage levels" to provide each needed on-board regulated voltage. *Id.* (alteration by Petitioner; emphasis omitted; citing Ex. 1023 ¶¶ 10, 12). Petitioner contends that a "buck converter" was a conventional device for implementing such a "voltage-reducing switching converter." *Id.* (emphasis omitted; citing Ex. 1030, 2:41–43). Although the claim states that a converter circuit generates the fourth voltage, Dr. Wolfe testifies that a buck converter would be an obvious way to implement a converter circuit. Ex. 1003 ¶ 286 (cited by Pet. 28, n.2). Petitioner further contends a buck converter would have been an obvious way to step down a higher input voltage of 12V to a lower output voltage of 3.5V or less, and that there would have been a reasonable expectation of success because buck converters were well-known switching devices commonly used to step down the voltage between input and output, as had long been taught in textbooks. *Id.* at 28–29 (citing Ex. 1003 ¶¶ 146–149, 236–237; Ex. 1058, 3, 5, 12–16; Ex. 1032, 161, 164; Ex. 1024, Fig. 6; Ex. 1050, 1:21).

Petitioner further notes that "*buck converters*" were well-known as a highly-efficient way to step down voltages without generating excess heat or requiring large cooling devices, providing further motivation to use buck converters. *Id.* at 29–30 (citing Ex. 1003 ¶ 237; Ex. 1040, 1, 23–24, Figs. 22–25; Ex. 1041, 1, 13; Ex. 1048, 3; Ex. 1058, 5; Ex. 1059, 5:23–30; Ex. 1062, 11; Ex. 1064 ¶ 101).

Additionally, Petitioner contends that it would have been obvious to use at least four converters in Harris given the need for four different voltages (e.g., 0.9V, 1.5V, 1.8V, 3.3V) in the FBDIMM Standards. *Id.* at 30

(citing Pet. 14–19). Petitioner asserts that it would have been obvious to use four converters because the voltages at the same level in Petitioner's voltage mappings A and B are described as separate voltages with separate pins that are separately controllable in the FBDIMM Standards. *Id.* at 30–31 (citing Ex. 1028, 17–20, 30–32; Ex. 1026, 2–3, 9; Ex. 1003 ¶¶ 242, 256; Ex. 1062, 13).

For the reasons discussed above in Section III.D.3, we disagree with Patent Owner's arguments regarding the use of buck converters.

Based on our review and consideration of the record, we determine that Petitioner has shown that the combination of Harris and the FBDIMM Standards teaches limitations 1.c to 1.f of claim 1.

> *d) Limitation 1.g: "a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:"*

Petitioner asserts that Harris discloses a "*a plurality of components coupled to the PCB*" including a Buffer and DRAMs shown in Harris's Figure 3, and a Serial Presence Detect (SPD) and resistors. Pet. 31 (citing Pet. 14–19; Ex. 1003 ¶¶ 288–90, 293–297). Petitioner further contends that

these components are each coupled to at least one or more of the second, third, and fourth regulated voltages. *Id.*

Patent Owner does not dispute that the combination of Harris and the FBDIMM Standards discloses this feature. *See* Resp.

Based on our review and consideration of the record, we determine that Petitioner has shown that the combination of Harris and the FBDIMMs Standards teaches this limitation.

> *e) Limitation 1.h: "a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and"*

Petitioner asserts that Harris discloses that the plurality of components includes a plurality of DDR DRAM devices 110-1 to 110-N as shown in Harris's Figure 1A and DRAM devices 312-1 to 312-8 for each of the memory modules shown in Harris's Figure 3. Pet. 32 (citing Ex. 1023 ¶¶ 9, 11, Figs. 1A, 3; Ex. 1003 ¶¶ 298–303). Petitioner contends that a person of ordinary skill in the art would have known that, according to the JEDEC standards, DDR memory devices are "synchronous" DRAM devices. *Id.* (citing Ex. 1026, cover; Ex. 1028, 9; Ex. 1045, cover; Ex. 1046, cover).

Patent Owner does not dispute that the combination of Harris and the FBDIMM Standards discloses this feature. *See* Resp.

Based on our review and consideration of the record, we determine that Petitioner has shown that the combination of Harris and the FBDIMMs Standards teaches this limitation.

f) Limitation 1.i.1: "at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices"

Petitioner contends that the "first circuit" corresponds to Harris's buffer 112 as shown in Harris's Figure 1A, as well as the buffer of memory module 306-1 in Harris's Figure 3. Pet. 32–34 (citing Pet. 20–25; Ex. 1023, Figs. 1A, 3; Ex. 1003 ¶¶ 304–317). Petitioner contends that Harris's buffers are coupled to receive data, address, and control signals via memory controller interface 114 across edge connections, and transmits them to DRAMs 110-1 to 110-N or DRAMs 312-1 to 312-8. *Id.*

Patent Owner does not specifically respond to Petitioner's contentions for this limitation. *See* Resp.

Based on our review and consideration of the record, we determine that Petitioner has shown that the combination of Harris and the FBDIMM Standards teaches this limitation.

g) Limitation 1.i.2: "the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices"

Petitioner relies on the same showing for limitation 1.i.2 as for limitation 1.i.1. Pet. 32–34.

For the reasons stated with respect to limitation 1.b, the combination of Harris and the FBDIMM Standards discloses this limitation notwithstanding Patent Owner's arguments. *See* Section III.D.4.b.2.

Based on our review and consideration of the record, we determine that Petitioner has shown that the combination of Harris and the FBDIMM Standards teaches this limitation for.

h) Limitation 1.i.3: "the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage"

Petitioner contends that Harris with the FBDIMM standards discloses this limitation. Pet. 34–35 (citing Pet. 14–19, 27; Ex. 1003 ¶¶ 318–323). Specifically, Petitioner contends that Harris's buffer 112 in Figure 1A is coupled to "the second regulated voltage" (e.g., V_{CC} or V_{CCFBD}=1.5V) and "the fourth regulated voltage" (e.g., V_{DDSPD}=3.3V). *Id.*

Patent Owner does not specifically respond to Petitioner's contentions for this limitation. *See* Resp.

Based on our review and consideration of the record, we determine that Petitioner has shown that the combination of Harris with the FBDIMM Standards teaches this limitation.

i) Limitation 1.i.4: "wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes."

Petitioner contends that "one of the second and fourth voltage[s]" (e.g., 1.5V) "is less than a second one of the second and fourth voltage[s]" (e.g., 3.3V). Pet. 35 (citing Pet. 14–19, 27; Ex. 1003 ¶¶ 324–327).

Patent Owner does not specifically respond to Petitioner's contentions for this limitation. *See* Resp.

Based on our review and consideration of the current record, we determine that Petitioner has shown that the combination of Harris with the FBDIMM Standards teaches this limitation.

j) Determination for Claim 1

Petitioner has shown that one of ordinary skill in the art would have had reason to combine Harris and the FBDIMM Standards with a reasonable

expectation of success. Petitioner has further shown that the combination of Harris and the FBDIMM Standards meets each limitation of claim 1. Accordingly, Petitioner has established by a preponderance of the evidence that claim 1 is unpatentable as obvious over the combination of Harris and the FBDIMM Standards.

5. Claims 2, 3, 8, 14, and 15

Claim 2 depends from claim 1 and recites "wherein the first and third buck converters are further configured to operate as a dual buck converter." EX. 1001, 38:53–55. Petitioner contends that the combination of Harris and the FBDIMM Standards discloses this limitation. Pet. 35–40. Specifically, Petitioner contends that at the time there were many commercially available products that could output two regulated voltages using buck converters, and thus, it would have been obvious to implement two or more of the regulated voltages such as the "first" and "third" voltages as a "dual buck converter" to reduce the number of integrated circuits, pins, and interconnections on the module, therefore simplifying the design. Pet. 36 (Ex. 1003 ¶ 338). Petitioner contends that commercially available devices included the Murata MPD4S014S dual buck converter (EX. 1042, 6; Ex. 1048, 1–2; Ex. 1058, 5), the Texas Instruments TPS51020 Dual Step-Down Controller (Ex. 1040, 1, 11) and the Fairchild Semiconductor FAN5026 Dual-Output PWM Controller" (Ex. 1041, 1, 2, 9). *See* Pet. 36–40.

Patent Owner presents no argument specific to claim 2. *See* Resp.

Based on our review and consideration of the current record, we determine that Petitioner has shown that the combination of Harris with the FBDIMM Standards renders claim 2 obvious.

Claims 3 depends from claim 1 and recites "wherein the first voltage amplitude is 1.8 volts." Ex. 1001, 38:56–57. Petitioner contends that the combination of Harris and the FBDIMM Standards discloses this limitation. Pet. 41 (citing Pet. 14–19, 27; Ex. 1003 ¶¶ 348–353).

Patent Owner presents no argument specific to claim 3. *See* Resp.

Based on our review and consideration of the record, we determine that Petitioner has shown that the combination of Harris with the FBDIMM Standards renders claim 3 obvious.

Claim 8 depends from claim 1 and recites

> the plurality of components further comprising:
> one or more registers coupled to one of the first, second, third and fourth regulated voltages, the one or more registers configured to register, in response to a clock, the first plurality of address and control signals, wherein the one of the first, second, third and fourth regulated voltages is selectively switched off to turn power off to the one or more registers while one or more components of the plurality of components are powered on.

Ex. 1001, 39:9–19.

Petitioner contends the combination of Harris and the FBDIMM Standards discloses claim 8. Pet. 41–46. Specifically, Petitioner contends that Harris's buffer 112 is a component that has registers to register incoming signals and output them according to a "clock" signal, as shown in Harris's Figures 1A and 3. *Id.* at 41. Petitioner contends Harris's buffer 112 is coupled to the voltage V_{CC} or V_{CCFBD} as the "second regulated voltage." *Id.* (citing Pet. 14–19, 27). Petitioner contends Harris discloses "buffer/logic component 112 is provided for buffering command/address (C/A) space as well as data," which a person of ordinary skill in the art would have understood involves registers for registering the address, control, and data

signals in response to a "clock" signal. *Id.* at 42 (citing Pet. 22–25; Ex. 1023 ¶¶ 9, 17, Fig. 3; Ex. 1003 ¶¶ 400–402; Ex. 1027, 19) (emphasis omitted).

Petitioner further contends that the combination of Harris and the FBDIMM Standards discloses an S3 sleep mode that selectively switches off the second voltage to turn off the power to the one or more registers while the DRAMs remain powered on to refresh data in the DRAMs. Pet. 45 (citing Pet. 14–19, 27; Ex. 1003 ¶¶ 410–411, 414–420; Ex. 1012 ¶ 9; Ex. 1027, 21, 39).

We have already addressed Patent Owner's arguments for patentability of claim 8 with respect to limitation 1.b and determine they do not undermine Petitioner's showing. *See* Section III.D.4.b.2.

.

Based on our review and consideration of the record, we determine that Petitioner has shown that the combination of Harris with the FBDIMM Standards renders obvious claim 8.

Claim 14 depends from claim 8 and recites

> wherein, in response to selectively switching on the one of the first, second, third and fourth regulated voltages to the one or more registers, the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices.

Ex. 1001, 39:40–45.

Petitioner contends that when the S3 sleep mode ends, normal DRAM transactions begin again and the second voltage which powers the input/output registers switches on and the registers output the registered address and control signals to the SDRAM devices. Pet. 46 (citing Ex. 1027, 25; Ex. 1003 ¶¶ 462–466).

For the reasons stated for claim 8, we determine that Patent Owner's arguments do not undermine Petitioner's showing. Resp. 11–15.[5]

Based on our review and consideration of the record, we determine that Petitioner has shown that the combination of Harris with the FBDIMM Standards renders claim 14 obvious.

Claim 15 depends from claim 1 and recites

> the plurality of components further comprising:
> a logic element including one or more integrated circuits and discrete electrical elements, the one or more integrated circuit including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information.

Ex. 1001, 39:46–52.

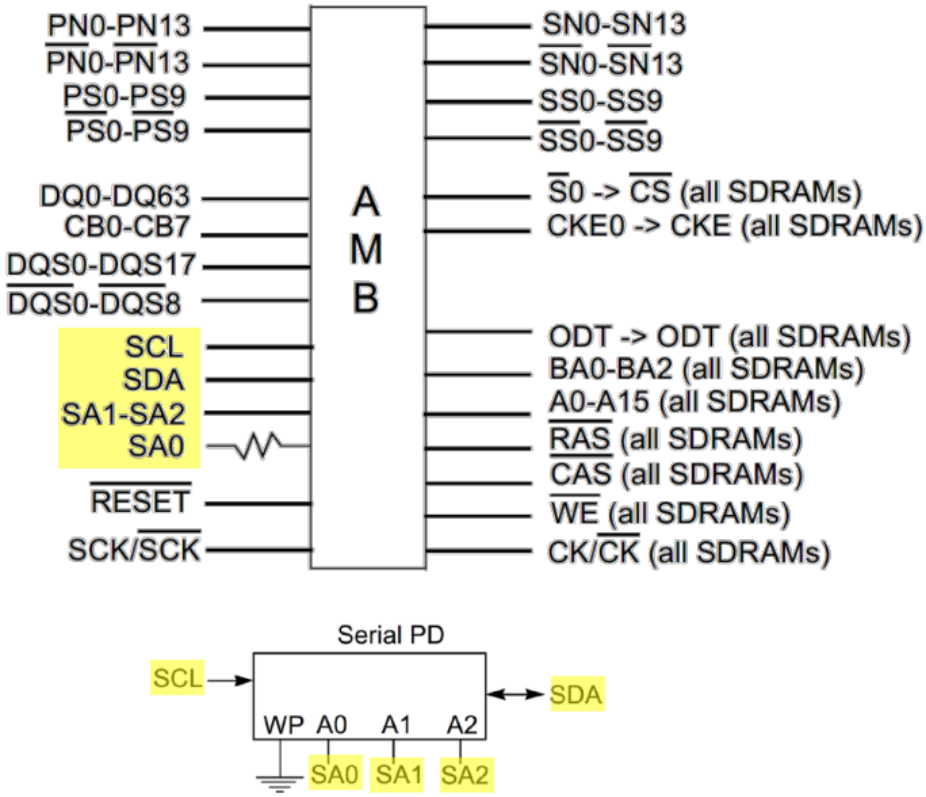
Petitioner contends that the combination of Harris and the FBDIMM Standards discloses claim 15. Pet. 47–50. Specifically, Petitioner contends logic in Harris's buffer includes an integrated circuit, as does its serial presence detect (SPD), including non-volatile memory. Pet. 47 (citing Ex. 1027, 25; Ex. 1003 ¶¶ 435–437, 468–476). Petitioner further contends the logic element includes discrete elements such as resistors and capacitors to terminate voltages for Harris's buffer. *Id.* Petitioner asserts that the S3 sleep mode of the FBDIMM Standards requires S3 Recovery Configuration Registers. *Id.* According to Petitioner, an FBDIMM like Harris's memory module will store configuration information in non-volatile memory before entering into S3 sleep mode. *Id.* (citing Ex. 1027, 25, 95–96, 141). Petitioner further contends that a person of ordinary skill in the art would

[5] Patent Owner makes this same argument for claim 21 challenged under Ground 2, which we find does not undermine Petitioner's showing for the same reasons as stated for claim 8. Resp. 11–15.

have understood that the "non-volatile memory" can be implemented in the SPD device separate from the integrated circuit implementing the AMB (Advanced Memory Buffer) where the SPD is used to store configuration information in the non-volatile memory. *Id.* at 48–49 (citing Ex. 1023 ¶ 19; Ex. 1027, 117; Ex. 1028, 13; Ex. 1066, 26:64–27:4; Ex. 1067, 1-1; Ex. 1003 ¶ 436). Petitioner further contends a person of ordinary skill in the art would have understood that the logic element includes discrete electrical elements such as resistors and capacitors, as taught by the FBDIMM Standards. *Id.* at 49–50 (citing Ex. 1003 ¶ 475; Ex. 1023 ¶ 9, Fig. 1A; Ex. 1028, 13, 42–45).

Patent Owner argues that Dr. Wolfe acknowledged that the AMB neither inherently nor expressly disclosed having a non-volatile memory. Resp. 43 (citing Ex. 2030, 285:23–286:17; *see also* Ex. 2031 ¶ 122); Sur-Reply 22. Patent Owner further argues that the statement in the FBDIMM Standards that the Control and Status Register (CSR) for the S3 sleep mode should be stored in non-volatile memory does not mean that the non-volatile memory is in the AMB. Resp. 43 (citing Ex. 2030, 285:23–286:17); Ex. 1003 ¶ 435 (CSR meaning). Patent Owner further notes that Dr. Wolfe stated that he had no knowledge that any AMB included a non-volatile memory. *Id.* (citing Ex. 2030, 292:10–20, 293:1–6). Patent Owner argues that the CSRs that the Petition references at page 47 are stored in volatile, not non-volatile, memory. *Id.* (citing Ex. 2030, 293:8–294:2). Patent Owner further argues that SPD and AMB are two different components. *Id.* (citing Ex. 2030, 293:1–6, 292:21–25). For these reasons, Patent Owner argues that Petitioner "has not cited any reference showing a logic element with a non-volatile memory." *Id.*

To explain his views, Dr. Wolfe reproduces the figure below from the FBDIMM Standards:



Ex. 1003 ¶ 437 (citing Ex. 1028, 13) (highlighting Dr. Wolfe's). Dr. Wolfe shows that the SPD is connected to the AMB to exchange the signals indicated in yellow highlighting. He further states that "the 'logic element' includes the logic in the buffer 112 and non-volatile memory (e.g., internal or external to the buffer) for storing configuration information as required by the S3 sleep mode." *Id.*

There is no dispute on this record that the SPD is non-volatile memory—the FBDIMM Standards require it to be. Ex. 1027, 25. Dr. Wolfe expounds that the SPD can contain non-volatile memory, such as an EEPROM, for storing configuration information using a higher voltage supply at 3.3V. Ex. 1003 ¶ 436. Dr. Wolfe stated that "it would have been

obvious to a [person of ordinary skill in the art] to implement the buffer 112 with an internal nonvolatile memory because it would decrease the number of components, interfaces and interconnections on the memory module, resulting in a cheaper, faster, and more secure solution." Ex. 1003 ¶ 436. Dr. Wolfe further states that the SPD and AMB are tied to the same voltage V_{DDSPD}. *Id.* In other words, the SPD and AMB are closely related.

Dr. Mangione-Smith states that the SPD and AMB are two different components. Ex. 2031 ¶ 123. The claims do not preclude, however, that the "logic element" may be parts of the SPD and AMB (Harris's FBDIMM buffer) related to the SPD functionality. Ex. 1023 ¶ 9; Ex. 1028, 105; 1003 ¶ 474. In fact, as Petitioner notes, claim 15 recites that the logic element may include "*one* ***or more*** integrated circuits." Reply 23 (citing Ex. 1001, 23:1–18; Pet. 47–49; Ex. 1003 ¶¶ 434–436). Accordingly, Petitioner has shown that the combination discloses a "logic element including a non-volatile memory" as claimed. Pet. 47–50, 67–68, 72; Reply 23.

There is no dispute that the CSRs, which are stored in the SPD before the memory module enters the S3 sleep mode, constitute "configuration information" as recited in claim 15. Pet. 47 (citing Ex. 1027, 25 (DRC, MTR, DREFTC, DAREFTC, S3RESTORE[15:0], SPDPAR[15:0] – SPDI personality bytes), 95–96, 141; Ex. 1003 ¶ 435)).

Further, there is no dispute that Harris's buffer and the SPD are "integrated circuits," and that the buffer is connected to "discrete electrical elements" (e.g., resistors and capacitors) as recited in claim 15. Ex. 1023, Figs. 1A, 3 (showing buffer is integrated circuit on DIMM); Ex. 1027, 25 (non-volatile memory is an integrated circuit); Ex. 1028, 43 (showing resistors and capacitors connected to AMB).

Thus, we agree with Petitioner that the features of these claims are taught or at least suggested by the combination of Harris and the FBDIMM Standards. Based on our review and consideration of the record, we determine that Petitioner has shown that the combination of Harris with the FBDIMM Standards renders claim 15 obvious.

6. Claim 23

Claim 23 is an independent claim. Ex. 1001, 40:50–41:21. Petitioner contends that the limitations of claim 23 are substantially identical to earlier limitations, and are thus obvious for the reasons stated above. Pet. 50–51.

Patent Owner presents no additional argument for claim 23 other than arguments previously discussed. *See* Resp.

Based on our review and consideration of the record, we determine that Petitioner has shown that Harris in combination with the FBDIMM Standards renders obvious claim 23.

7. Determination for Ground 1

Petitioner has shown by a preponderance of the evidence that claims 1–3, 8, 14, 15, and 23 are unpatentable as obvious over the combination of Harris and the FBDIMM Standards for the reasons explained.

E. Ground 2: Obviousness Over Harris, the FBDIMM Standards, and Amidi

Petitioner contends that claims 1–30 of the '918 patent would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi. Pet. 51–75. For the reasons that follow, we are persuaded that the evidence, including Dr. Wolfe's testimony, sufficiently supports Petitioner's arguments and, therefore, establishes by a preponderance of the evidence

that claims 1–30 of the '918 patent are unpatentable as obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

1. Amidi (Ex. 1024)

Amidi was filed on October 25, 2006, issued on May 25, 2010, and is titled "Clock and Power Fault Detection for Memory Modules." Ex. 1024, codes (22), (45), (54). Petitioner contends Amidi is prior art under § 102(e). Pet. 12.

Amidi's Figure 5 is reproduced below.

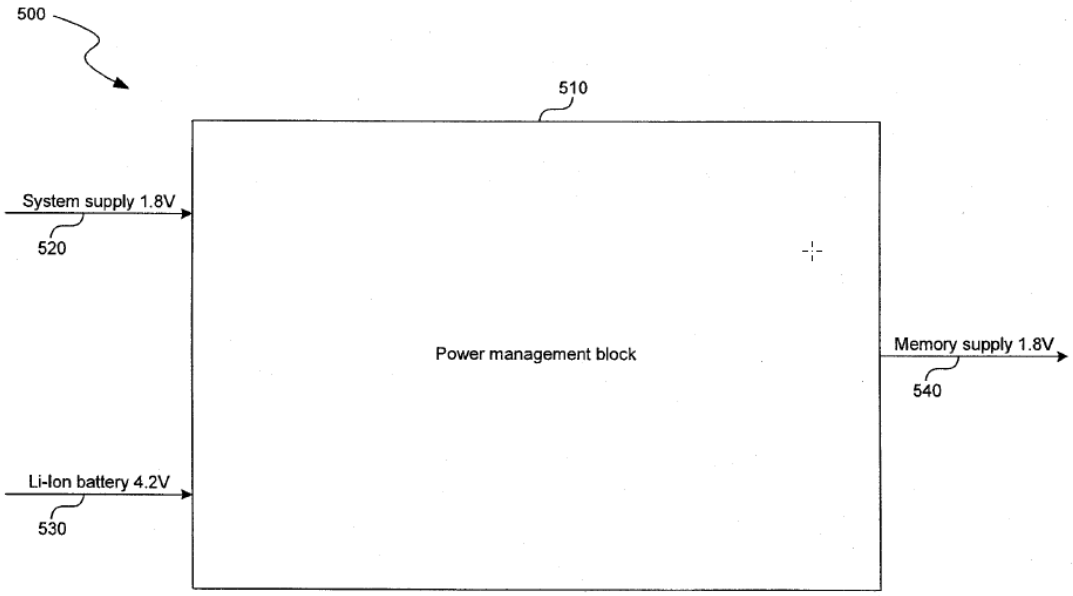


FIG. 5

Amidi's Figure 5 above illustrates a power management block 510 that receives an incoming system supply 520, and incoming battery supply 530, and generates an outgoing memory power supply 540 that is stabilized in the face of disruptions to the system supply 520 using the battery supply 530. Ex. 1024, 4:14–22, 8:23–36, Figs. 5, 14; Ex. 1003 ¶¶ 131–132.

2. Motivation to Combine

Petitioner contends that a person of ordinary skill in the art would have been motivated to combine Harris and the FBDIMM Standards with Amidi with a reasonable expectation of success. Pet. 52. Specifically, Petitioner contends that Harris recognizes concerns with power reliability and proposes the use of a redundant power source. *Id.* (citing Ex. 1023 ¶¶ 12–14, 16, Figs. 1B, 2). Petitioner notes that Amidi teaches a redundant power source (a battery on the memory module) for maintaining data during power disruption. *Id.* at 52–53 (citing Ex. 1024, code (57), 1:28–35, 2:6–26, 4:14–60, Figs. 5–6; Ex. 1003 ¶¶ 170–175). Petitioner further notes that Amidi's power management block could be modified easily to work with Harris's FBDIMM memory module by changing the system supply 520 and memory supply 540 to 12V as taught by Harris. *Id.* at 53 (citing Ex. 1024, Figs. 5, 6; Ex. 1023 ¶ 12; Ex. 1003 ¶¶ 171–172). Petitioner contends that, to a person of ordinary skill in the art, it would have been obvious to use the 12V external supply stepped-down with a buck converter to a 5V supply for charging Amidi's battery, and that Amidi's battery voltage would be stepped-up with a boost converter to the 12V level used by Harris's memory module. *Id.* at 53–54 (citing Ex. 1024, Fig. 6 (620); Ex. 1003 ¶¶ 171–172). Petitioner contends that Amidi discloses that its power management block uses "buck" converters to step-down voltages as needed, and "boost" converters to step-up voltages as needed, as had long been taught in textbooks. *Id.* at 54 (citing Ex. 1024, 4:27–32, 4:38–40, Figs. 5, 6; Ex. 1058, 3; Ex. 1032, 161). Petitioner further contends that Amidi's battery backup mode is similar to the S3 power-saving mode of Harris's FBDIMM memory module and the FBDIMM Standards, such that a person of ordinary skill in

the art would have been motivated to combine their teachings. *Id.* at 54–56. Petitioner contends this is a straightforward modification of Harris's memory module in view of Amidi and the knowledge of a person of ordinary skill in the art and simply uses a known technique (e.g., Amidi's battery backup techniques) to improve a similar device (e.g., Harris's memory module) in the same way (e.g., to provide a backup power supply using a battery). *Id.* at 55 (citing Ex. 1003 ¶ 175). In addition, Petitioner contends, the modification merely applies a known technique (e.g., providing a backup power supply) to a known device (e.g., a memory module) that is ready for the improvement to yield predictable results (e.g., redundancy when the system supply or clock fails). *Id.*

Petitioner contends that the combination of Harris, the FBDIMM Standards, and Amidi would result in the following configuration and voltage mappings:

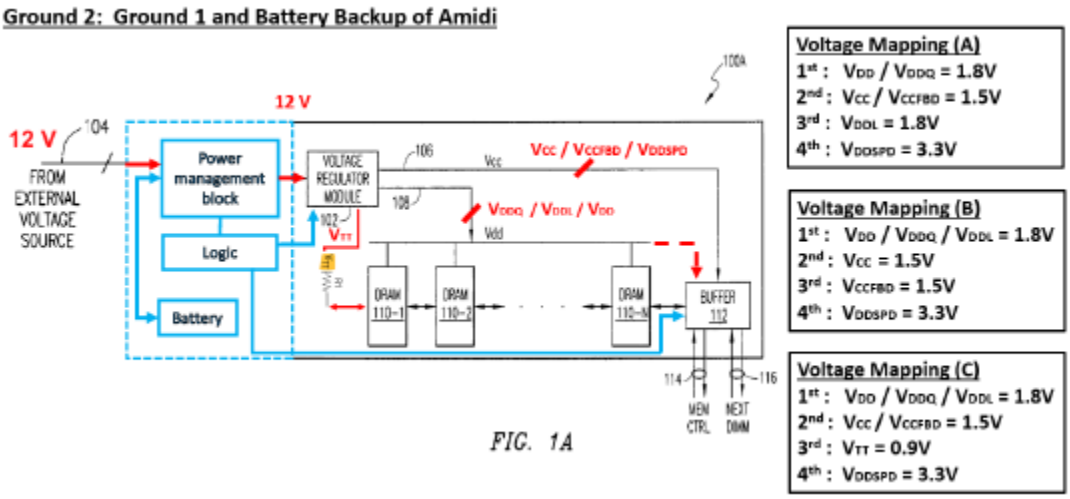


FIG. 1A

Pet. 55–56 (citing *id.* at 14–19, 27; Ex. 1003 ¶¶ 174–179). Above, Petitioner has annotated Harris's Figure 1A to show features added from the teachings

of the FBDIMM Standards (red) and features added from the teachings of Amidi (blue). *Id.*

Patent Owner argues that Harris provides alternate voltage sources to power a memory module in the event of a power interruption, so Harris already provides a solution for the alleged problem that Amidi addresses. Resp. 31–38; Sur-Reply 19–20. Specifically, Patent Owner argues that Harris has "logic 124" that selects a different voltage source if power becomes unavailable on one of the supply voltage paths 120-1 through 120-K. Resp. at 32–33 (citing Ex. 1023, Fig. 1B; Ex. 2031 ¶ 106). Patent Owner further argues that substituting Amidi's battery backup solution for Harris's redundant power sources would require substantial space to accommodate the lithium battery and associated battery charging and monitoring circuits and power management block. *Id.* at 35–38 (citing Ex. 1024, Figs. 4–6; Ex. 1023 ¶¶ 2, 13; Ex. 2031 ¶¶ 108 n.5, 109). Patent Owner argues that Petitioner "has entirely ignored the issue of whether the essential parts of Amidi it seeks to apply to the combination would even fit onto Harris' circuit board" and that "Petitioner has presented no evidence that a [person of ordinary skill in the art] would expect Harris' memory module to be able to accommodate three buck converters, a lithium battery and its associated charging and monitoring circuits, and Amidi's power management module, at least not without undergoing a substantial re-design." *Id.* at 35–38 (citing Ex. 1055, Fig. 4; Ex. 2101, 20; Ex. 2042, 7; Ex. 2031 ¶ 112).

We agree with Petitioner that Amidi provides a redundant power supply on the memory module that is independent from the host, and that a person of ordinary skill in the art would have seen the value of adding a

redundant power supply onboard Harris's memory module at least for some practical applications. Reply 19–20 (citing Pet. 52–53; Ex. 1003 ¶ 170; Ex. 1024, 1:28–35, 2:6–26). Although Harris mentions an "external voltage source," it does not mention the term "battery." Hence, Patent Owner's arguments that Amidi provides a solution to a problem that Harris already solves is not correct. *See* Ex. 1003 ¶ 170 ("Amidi recognizes that it is useful to keep data on the memory module with a backup power supply on the module itself, such as a battery supply, when the entire system surrounding the memory module loses power.") (citing Ex. 1024, 1:28–35; 2:6–26). Furthermore, Petitioner shows that memory modules with battery backup were known in the art and readily available. Reply 19 (citing Ex. 2035, 39; Ex. 1075, 165:10–167:7). As to the space issue, Petitioner notes that even if the battery backup occupies one side of an FBDIMM board, the other side still can include one rank or two ranks using stacked memory devices. *Id.* at 19–20 (Ex. 1028, 36; Ex. 1075, 74:22–75:25, 77:10–17).

Accordingly, we determine that Petitioner has shown that one of ordinary skill in the art would have been motivated to combine Harris, the FBDIMM Standards, and Amidi with a reasonable expectation of success.

3. Claims 1–3, 8, 14, 15, and 23

We agree with Petitioner that the addition of Amidi does not negate Petitioner's showing with respect to the previous ground. Pet. 56, 66–67 (citing Ex. 1003 ¶¶ 215–353, 412–413, 467–476, 557–597). Accordingly, Petitioner has shown by a preponderance of the evidence that claims 1–3, 8, 14, 15, and 23 are unpatentable as obvious over the combination of Harris, the FBDIMM Standards, and Amidi for the reasons stated in the previous ground.

4. Claims 16–22 and 30 ("pre-regulated input voltage")

Claims 16–22 and 30 recite a "pre-regulated input voltage." Ex. 1001, 39:61, 42:23. As explained in Section III.C.2, we understand "pre-regulated input voltage" to mean that the voltage is regulated before conversion to a stepped up or down level by the voltage converters. *See* Ex. 1001, code (57), 28:53–58, Fig. 16 (1110, 1112).

Petitioner contends that, with the exception of the "pre-regulated input voltage" limitation, claims 16–22 and 30 are combinations of limitations previously discussed which are rendered obvious for the reasons for reasons earlier presented in the Petition. Pet. 70–75. Petitioner provides a table showing the correspondences of the limitations of these claims to others discussed earlier in the Petition. *Id.* at 71–73. We agree that each limitation of these claims is taught or suggested by the combination of Harris, the FBDIMM Standards, and Amidi for the reasons previously discussed in the Petition for those same limitations.

Turning to the "pre-regulated input voltage" limitation, Petitioner contends that Harris discloses an input that is "pre-regulated" because it is "within pre-determined limits" and because it can be "regulated." Pet. 73 (citing Ex. 1023 ¶¶ 13–14; Ex. 1003 ¶¶ 487–488). Alternatively, Petitioner contends that Amidi teaches a boost converter in its power management block that converts (and thus pre-regulates) the battery voltage to an output of 12 Volts. Pet. 73–74 (citing *id.* at 52–56; Ex. 1003 ¶ 489; Ex. 1032, 161 (explaining that switch-mode converters, including boost converters, "convert the unregulated dc input into a controlled dc output at a desired voltage level")).

Patent Owner states that Harris's 12V input with a "+/-15%" tolerance is an unregulated voltage source. Resp. 38 (citing Ex. 1023 ¶ 13). Patent Owner does not explain what distinguishes a regulated voltage from an unregulated one, but, in any event, Harris expressly discloses that the external voltage supply may be "regulated." Ex. 1023 ¶ 14. This means "pre-regulated" in the context of the claims. Pet. 73–74 (citing Ex. 1023 ¶¶ 13–14; Ex. 1003 ¶¶ 487–489). Because the voltage that is received at the voltage converters has already been regulated externally, this meets our adopted construction (which, as we note above, is consistent with Patent Owner's proposed construction). *See* Resp. 38 ("A pre-regulated input voltage is just a regulated voltage provided to these voltage conversion circuits.").

Patent Owner further argues that "when a power supply other than the 12V external power source is used, Harris teaches the use of corresponding VRMs." Resp. 38 (citing Ex. 1023 ¶ 14, Fig. 1B). Therefore, Patent Owner argues, there is no reason to generate a pre-regulated 12V voltage, as Petitioner contends. *Id.* But, as explained, Harris expressly discloses that a "regulated" voltage may be input to its memory module and, therefore, Harris teaches converters that are "configured to receive a pre-regulated input voltage," as recited in the claims. Ex. 1023 ¶ 14.

After reviewing the record, we determine that Petitioner has shown by a preponderance of the evidence that the combination of Harris, the FBDIMM Standards, and Amidi teaches the "pre-regulated input voltage" subject matter of claims 16–22.

5. Claims 5–7, 9–13, 16–22, and 24–27

Claims 5–7, 9–13, 16–22 and 24–27 recite, or depend from a claim that recites, that the voltage monitor circuit generates the trigger signal in response to the input voltage being ***greater than*** a predetermined threshold voltage. Ex. 1001, 38:61–67, 40:7–13, 41:22–27, 42:21–26. Claims 11, 12, 18, 19, 25, and 26 require certain actions to be taken in response to the "trigger signal."

a) Trigger Signal on Overvoltage—Claims 5, 16, and 24

Claim 5 recites

> a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage.

Ex. 1001, 38:61–67. Claims 16 and 24 recite similar limitations. *Id.* at 41:22–27, 40:7–12.

We address claim 5 as representative of this group of claims. For claim 5, Petitioner contends that Harris teaches detecting both undervoltage and overvoltage conditions. Pet. 62 (citing Ex. 1023 ¶ 13). In this regard, Harris states that the tolerance of the +12V power supply is "around +/- 15%." Ex. 1023 ¶ 13. Petitioner asserts that, in the combination, Amidi's power supervisory module/block 665 ("voltage monitor circuit") monitors system supply 605 ("power input voltage") received from Harris's edge connections. Pet. 60–61 (citing Ex. 1003 ¶¶ 359–376). Petitioner further asserts that Amidi's signal 670 is the claimed "trigger signal" to switch to battery power. *Id.* at 61–62 (Ex. 1024, 4:44–52, 5:25–43, 8:23–29, 9:8–12, Figs. 5, 6, 14–15). Petitioner contends that such circuitry for either

overvoltage and undervoltage protection was well known and commercially available. *Id.* at 62–63 (citing Ex. 1063, 1–2; Ex. 1061, 15 (circuit for "undervoltage" and "overvoltage" detection); Ex. 1062, 15 (same); Ex. 1065, code (57), ¶¶ 14, 18–19, Figs. 1, 5 (similar)).

Patent Owner argues that neither Harris nor Amidi teaches detecting an overvoltage. Resp. 39; Sur-Reply 20–22. However, Harris discloses that its +12V power supply has a tolerance of "+/- 15%" which indicates it would be a concern if the power supply was greater than 15%. Ex. 1023 ¶ 13. Amidi indicates concern with "power fault[s]." Ex. 1024, codes (54), (57). Although Patent Owner points out that Amidi discloses detection of undervoltage (Ex. 1024, Fig. 14), "power fault" is broad enough to encompass overvoltage as well. We agree with Petitioner that a person of ordinary skill in the art considering these teachings would have considered it obvious to detect overvoltage and generate a trigger signal in response to the detection.

Patent Owner argues that the voltage regulators on which Petitioner relies do not detect input overvoltage because they can accommodate a wide range of input voltages, and there is a low probability that they would exceed their operational range. Resp. 40 (citing Ex. 2030, 58:24–61:12; Ex. 1040; Ex. 1041; Ex. 2031 ¶ 117). Petitioner replies that power surges were a known problem that could cause data loss or corruption or damage circuitry in memory boards. Reply 21–22 (citing Ex. 1003 ¶¶ 371–373; Ex. 2030, 254:24–256:11, 258:12–20; Ex. 1065, 18–19; Ex. 1063, 1–2; Ex. 1061, 15; Ex. 1062, 15; Ex. 1075, 196:10–197:13). Petitioner contends that Harris discloses that its module can accommodate only "+/- 15%" of the

nominal supply voltage, which is consistent with maximum ratings for commercial converters. *Id.* at 22 (citing Ex. 1041, 4).

We agree with Petitioner that power surges would have been a problem in at least some circumstances for which one of ordinary skill in the art would have seen the value of voltage detection in order to take preventive action to avoid loss of data and damage to the memory module. Dr. Wolfe credibly explains that overvoltage was a danger known to persons of ordinary skill in the art, citing industry datasheets that specify overvoltage parameters. Ex. 1003 ¶¶ 371–373 (citing Ex. 1063, 1–2; Ex. 1061, 15; Ex. 1062, 15). Indeed, the cited evidence uses the phrase "an overvoltage fault" (Ex. 1061, 15), which shows that power faults are not limited to undervoltage situations.

b) Logic Element with Non-Volatile Memory—Claims 10, 11, 15, and 22

Claims 10, 11, 15, and 22 recite a logic element that includes a non-volatile memory. Ex. 1001, 39:23–27, 39:28–30, 39:46–52, 40:43–49. Claim 10 further recites that the non-volatile memory is "configured to store configuration information." Claim 11 depends from claim 10 and recites that the logic element writes information into the non-volatile memory in response to the trigger signal. Claim 15 further recites that logic element includes one or more integrated circuits including an internal non-volatile memory, and discrete electrical elements. Claim 22 omits mentions of integrated circuits or discrete elements, but recites that the configuration information is used to program the logic element.

Petitioner contends that the combination of Harris, the FBDIMM Standards, and Amidi discloses these claims. Pet. 47–50, 67–68, 72; Reply

23. Specifically, Petitioner contends that the "non-volatile memory" for the "logic" can be either in Harris buffer (e.g., an AMB) or in an SPD connected to that buffer. Pet. 47–50, 67–68, 72.

Patent Owner argues that the FBDIMM AMB is not disclosed as having a non-volatile memory, and that, although the SPD contains a non-volatile memory according to the FBDIMM standards, the AMB and SPD are two different components. Resp. 43.

For the reasons explained for claim 15 under Ground 1, Patent Owner's arguments do not undermine Petitioner's showing. Thus, we agree with Petitioner that the features of these claims are taught or at least suggested by the combination of Harris, the FBDIMM Standards, and Amidi.

c) Write Operation on Overvoltage—Claims 11, 12, 18, 19, 25, and 26

Claim 11 recites "wherein, in response to the trigger signal, the logic element writes information into the non-volatile memory." Ex. 1001, 39:28–30. Claim 12 depends from claim 11 and recites a non-volatile memory and a controller, and the controller performs a write operation to the non-volatile memory in response to the trigger signal. *Id.* at 39:31–39. Claim 18 recites a controller that executes a write operation in response to a (trigger) signal. *Id.* at 40:17–21. Claim 19 recites that the write operation includes writing data information into non-volatile memory. *Id.* at 40:22–24. Claim 25 recites a controller that executes a write operation in response to the trigger signal. *Id.* at 42:1–5. Claim 26 recites that the write operation includes writing data information to non-volatile memory. *Id.* at 42:6–8.

For claim 11, Petitioner contends that the trigger signal was explained with respect to claim 5 and may be a power disruption. Pet. 68. Petitioner further contends that the logic element writes S3 configuration information as discussed for claims 10 and 15, to allow sleep mode to conserve power during Amidi's battery backup mode. *Id.* (citing Ex. 1003 ¶¶ 439–443). Petitioner contends that Amidi's battery backup mode is similar to the S3 power-saving mode of Harris's FBDIMM memory module, because both modes put the SDRAMs in a self-refresh state to preserve data while conserving power. *Id.* (citing Pet. 45–46; Ex. 1024, 2:16–19, Fig. 11). In the event of a power disruption causing a trigger signal, Petitioner contends that a person of ordinary skill in the art would have been motivated to use the S3 sleep mode (Pet. 45–46) to conserve power during Amidi's battery backup mode, as discussed in claims 10 (Pet. 67) and 15 (Pet. 47–50), and that the S3 sleep mode requires writing S3 configuration information into the non-volatile memory in the SPD before going to sleep. *Id.* (citing Ex. 1003 ¶ 442). For claim 12, Petitioner contends that the "controller" corresponds to Harris's buffer, which stores S3 configuration information in non-volatile memory in the SPD before entering S3 sleep mode. Pet. 47–50, 67–68; Ex. 1071, 39–46; Ex. 1073, 46–63; Ex. 1003 ¶¶ 444–456. Petitioner relies on similar disclosures for claims 18, 19, 25, and 26. Pet. 71–73.

Patent Owner argues that S3 sleep mode is a low power state mode whereas overvoltage does not result in low or lost power. Resp. 44 (citing Ex. 2031 ¶ 124); Sur-Reply 22–23. Patent Owner also argues that known converters could operate even at high input overvoltage. Resp. 44 (citing Resp. Sect. IV.F.1).

Petitioner counters that overvoltage conditions can cause data loss, thus motivating a person of ordinary skill in the art to switch to backup power, where the S3 mode would be used. Reply 23 (citing Pet. 68–69).

Patent Owner argues that a memory module cannot decide to enter the S3 sleep mode upon detection of an overvoltage. Sur-Reply 22. Instead, according to Patent Owner, the CPU determines when the memory module should enter the S3 sleep mode. Sur-Reply 22–23 (citing Ex. 2030, 282:22–284:25; Ex. 2031 ¶¶ 124–125; Ex. 2006, 3). Patent Owner argues there is no evidence that such a modification could be predictably made or result in an operable implementation. *Id.* at 23 (citing Ex. 2031 ¶ 125).

As Petitioner notes, Amidi provides the teaching of generating the trigger signal ***onboard the memory module*** in response to detecting a "power fault" or "disruption." Pet. 12, 52, 55, 61–62; Ex. 1003 ¶¶ 132, 171, 174, 368–374. Considering the prior art teachings together, we agree with Petitioner that one of ordinary skill in the art would have understood that overvoltage detection and generating the trigger signal onboard the memory module was an option to pursue. This option would have been both predictable and pursued with a reasonable expectation of success since the prior art combination, Amidi in particular, teaches how it could be implemented.

6. Claims 4, 28, and 29

Claim 4 recites that the second, third, and fourth voltage amplitudes are 2.5V. 1.2V, and 3.3V, respectively. Ex. 1001, 38:58–60. Petitioner contends that Harris discloses voltages within the range of 0.5V to 3.3V, and that Voltage Mapping D from the FBDIMM Standards discloses these voltages. Pet. 57–60.

Claim 28 recites that the second and third buck converters are configured to operate as a dual buck converter. Ex. 1001, 42:14–16. Petitioner contends this feature is disclosed by the combination. Pet. 73.

Claim 29 recites that the SDRAMS devices are configured to receive one of the first through fourth regulated voltages at 1.8V. Petitioner contends this feature is disclosed by the combination. *Id.*

Patent Owner presents no arguments specific to these claims. Petitioner has shown that these claims are disclosed by the combination.

7. Determination for Ground 2

Petitioner has demonstrated that a person of ordinary skill in the art would have had reason to combine Harris, the FBDIMM Standards, and Amidi with a reasonable expectation of success. Petitioner has also demonstrated that all of the limitations of claims 1–30 are taught or suggested by the combination. Accordingly, Petitioner has demonstrated by a preponderance of the evidence that claims 1–30 of the '918 patent would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

F. Ground 3: Obviousness over Harris, the FBDIMM Standards, Amidi, and Hajeck

Petitioner contends claims 1–30 would have been obvious over the combination of Harris, the FBDIMM Standards, Amidi, and Hajeck. Pet. 75–77.

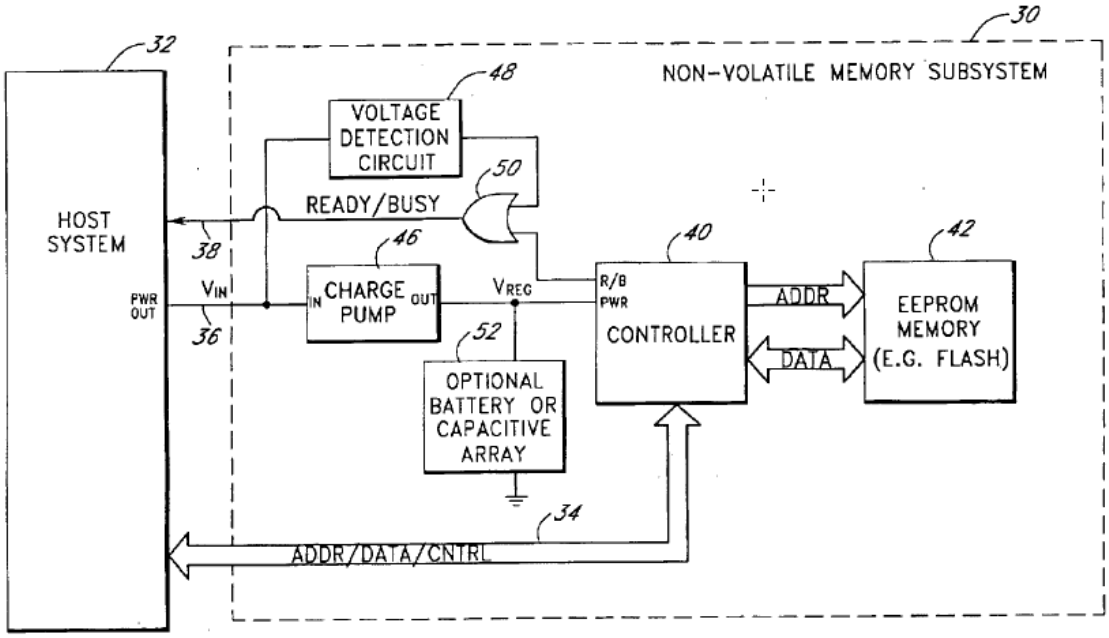
1. Hajeck (Ex. 1038)

Hajeck is titled "Storage Subsystem with Embedded Circuit for Protecting Against Anomalies in Power Signal from Host." Ex. 1038, code

(54). Hajeck issued as U.S. Patent No. 6,856,556 B1 on February 15, 2005. Petitioner contends Hajeck is prior art under § 102(b). Pet. 12.

Hajeck seeks to protect storage subsystems from damage and data loss caused by irregularities in a power signal provided by a host. Ex. 1038, 1:10–13. Specifically, Hajeck seeks to prevent data loss due to loss of power from a host system, and to prevent power surges or spikes from damaging circuitry of the storage subsystem. *Id.* at 1:15–31.

Hajeck's Figure 1 is reproduced below.



In Hajeck's Figure 1, non-volatile memory subsystem 30 receives power from host system 32 at charge pump 46 which supplies regulated voltage to controller 40. *Id.* at 2:64–67. In the event of a power surge or spike, charge pump 46 protects controller 40 from damage. *Id.* at 3:12–16. In the event of a voltage drop, charge pump 46 with battery and capacitive array 52 provides sustained voltage to controller 40. *Id.* at 2:60–63, 3:10–13. Voltage detection circuit 48 detects anomalies in the input voltage, including

undervoltage and overvoltage conditions, and generates a "busy" signal provided to the host system 32 to block the host system from performing write operations to the storage subsystem. *Id.* at 1:64–67, 3:30–43.

2. Motivation to Combine

Petitioner contends that one of ordinary skill in the art would have been motivated to combine Hajeck with Harris, the FBDIMM Standards, and Amidi because such person would have appreciated the desirability of switching to backup power in both undervoltage and ***overvoltage*** conditions. Pet. 75–76. Hajeck teaches to use a backup power supply, such as a charge pump, battery, or capacitive array, in response to power loss from the host system to complete outstanding operations, and to use the charge pump to protect the controller from surges or spikes in the power supply. *See, e.g.*, Ex. 1038, code (57), 1:53–61.

Petitioner also contends that overvoltage caused by anomalies such as power surges "can cause data loss, data corruption or circuitry damage in memory boards—as anyone with a surge protector at home knows." Reply 22 (citing Pet. 75–76; Ex. 1003 ¶¶ 137, 184). Although Patent Owner argues that Hajeck's charge pump protects against power surges (Resp. 41), Petitioner relies on Hajeck for its "teachings related to overvoltage anomalies when implementing Amidi's voltage supervisory block in Ground 2 so that it detects both undervoltage and overvoltage anomalies." Pet. 76 (emphasis omitted) (citing Ex. 1003 ¶¶ 185–187).

We agree with Petitioner that Patent Owner's arguments attack the references individually and do not properly consider what the combination of references would have signified to a person of ordinary skill in the art. Reply 21 (citing Resp. 39–42); *In re Merck & Co.*, 800 F.2d 1091, 1097

(Fed. Cir. 1986) (citing *In re Keller*, 642 F.2d 413, 425 (CCPA 1981)). Petitioner relies on Hajeck for its teaching of detecting an overvoltage condition to the extent that the combination of Harris, the FBDIMM Standards, and Amidi were deemed not to already disclose that feature. Pet. 76–77. Thus, the features that Patent Owner argues are missing from Hajeck are not ones for which Petitioner relied on Hajeck.

For similar reasons, we also do not agree with Patent Owner's argument that Hajeck does not suggest that data loss was a concern because its charge pump could provide the desired V_{REF} indefinitely. Resp. 42 (citing Ex. 2031 ¶¶ 120–121). Petitioner does not rely on Hajeck for its teaching of a charge pump, nor does Petitioner propose that one is included in the prior art combination. Pet. 75–76. In any case, Hajeck teaches that the charge pump provides power to its storage subsystem ***temporarily*** and that a battery or capacitive array may provide additional sources of backup power, so we do not agree that Hajeck teaches that the charge pump can supply power indefinitely. Ex. 1038, 1:56–61. Petitioner relies on Amidi for switching operational states and the voltage supply to battery backup in the event of an overvoltage. Reply 21 (citing Pet. 49–50). Thus, this argument too considers Hajeck individually, and not in combination with Harris, the FBDIMM Standards, and Amidi, as set forth in the Petition.

3. Overvoltage—Claims 5, 16, and 24

Claims 5, 16, and 24 recite detecting that the voltage monitor circuit is configured to produce a trigger signal in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage. Ex. 1001, 38:61–67, 40:7–12, 41:22–28. Petitioner contends that these claims are disclosed by the combination of Harris, the FBDIMM Standards,

Amidi, and Hajeck. Pet. 76–77. Patent Owner argues that these claims are not disclosed. Resp. 40–42.

Patent Owner argues that Hajeck does not teach a voltage detection circuit that produces a trigger signal that causes transitions to a different operable state or otherwise relates to switching power sources. Resp. 40–42 (citing EX1038, 3:6–10, 3:30-57, 3:66–4:9, Ex. 2031 ¶¶ 119–121). This attacks Hajeck individually and is an improper approach to the obviousness analysis. *See Merck, Keller, supra*. Petitioner relies on Hajeck for its teaching of detecting an overvoltage condition, in combination with the teachings of Harris, the FBDIMM Standards, and Amidi which teach the voltage detection circuit configured to produce the trigger signal. Pet. 12–13, 60–66, 75–77; Ex. 1003 ¶¶ 137, 180–87, 363–84; Ex. 2030, 226:16–22, 230:17–232:6, 251:10–254:2.

Accordingly, the combination of Harris, the FBDIMM Standards, Amidi and Hajeck teaches, or at least suggests, the limitations of claims 5, 16, and 24.

4. Remaining Claims

We find no reason suggesting that Hajeck would negate any of the teachings of Harris, the FBDIMM Standards, and Amidi as shown under Ground 2 (Sect. III.E). Thus, the combination of Harris, the FBDIMM Standards, Amidi, and Hajeck teach or suggest the limitations of the remaining claims under this Ground 3 for the same reasons stated for Ground 2.

5. Determination for Ground 3

Petitioner has shown that a person of ordinary skill in the art would have been motivated to combine Harris, the FBDIMM Standards, Amidi,

and Hajeck with a reasonable expectation of success. Petitioner also shows that each limitation of claims 1–30 is taught or at least suggested by the prior art combination. Accordingly, Petitioner has shown by a preponderance of the evidence that claims 1–30 are unpatentable as obvious over the combination of Harris, the FBDIMM Standards, Amidi, and Hajeck.

G. Grounds 4 and 5: Obviousness over Spiers and Amidi

As we have determined that claims 1–30 are unpatentable as obvious under Grounds 1 to 3, we do not reach Grounds 4 and 5.

H. Motion to Exclude

Petitioner seeks to exclude materials referenced in three URLs submitted with Patent Owner's Sur-Reply on August 4, 2023. Paper 33 (citing Paper 31, 1 n.2, 24, 26). Because we do not rely on any of these URLs in a manner adverse to Petitioner, we dismiss the Motion to Exclude as moot.

IV. CONCLUSION

For the foregoing reasons, we determine that Petitioner establishes by a preponderance of the evidence that claims 1–30 of the '918 patent are unpatentable.

V. ORDER

Accordingly, it is:

ORDERED that claims 1–30 of the '918 patent have been shown to be unpatentable;

FURTHER ORDERED that Petitioner's Motion to Exclude is dismissed as moot;

FURTHER ORDERED that any party seeking judicial review must

comply with the notice and service requirements of 37 C.F.R. § 90.2.[6]

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not shown Unpatentable
1–3, 8, 14, 15, 23	103	Harris, FBDIMM Standards	1–3, 8, 14, 15, 23	
1–30	103	Harris, FBDIMM Standards, Amidi	1–30	
1–30	103	Harris, FBDIMM Standards, Amidi, Hajeck	1–30	
1–30	103	Spiers, Amidi		
1–30	103	Spiers, Amidi, Hajeck		
Overall Outcome			1–30	

[6] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this Decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

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